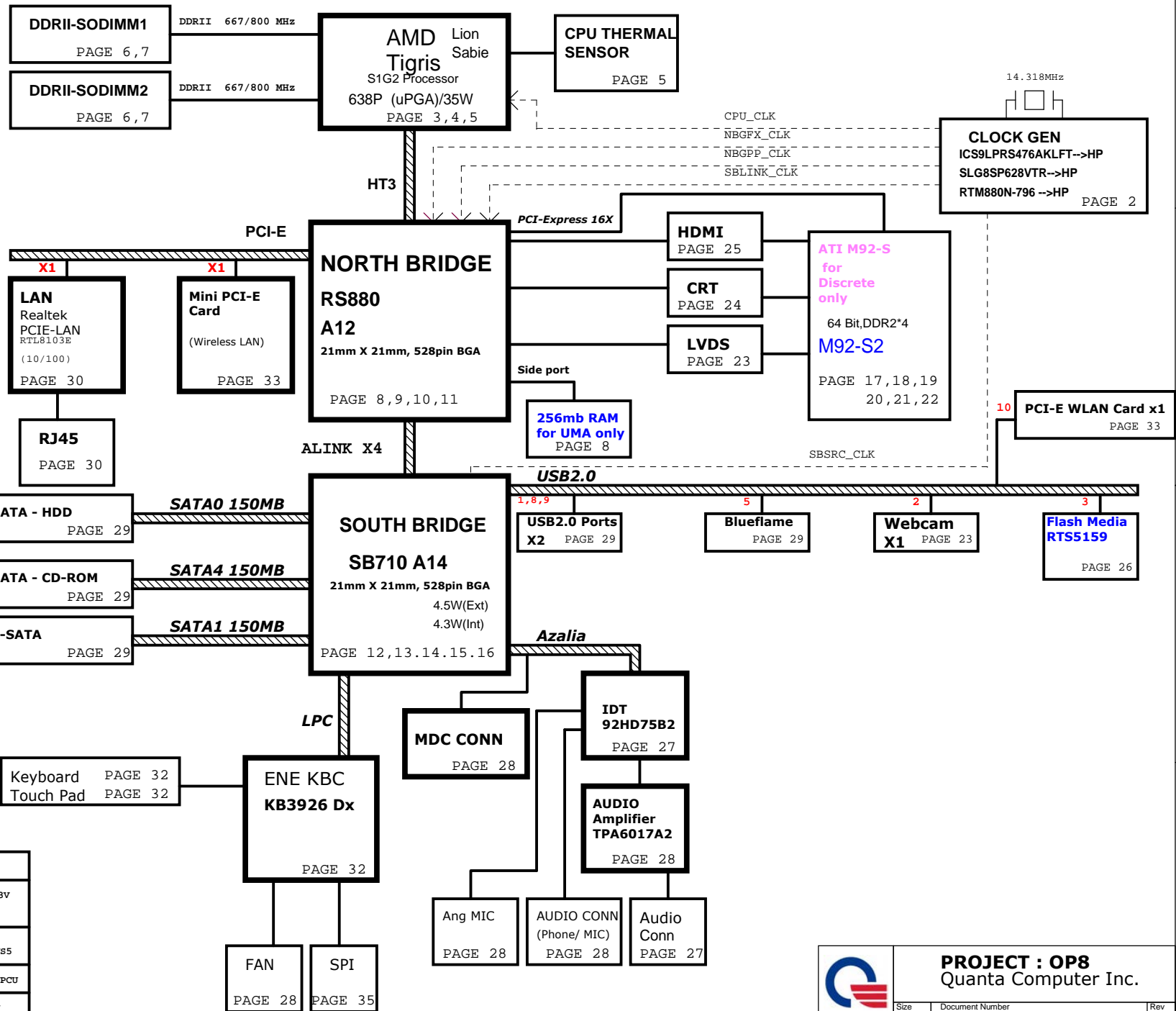


## PCB STACK UP

LAYER 1 : TOP  
LAYER 2 : IN1  
LAYER 3 : IN2  
LAYER 4 : VCC  
LAYER 5 : IN3  
LAYER 6 : BOT

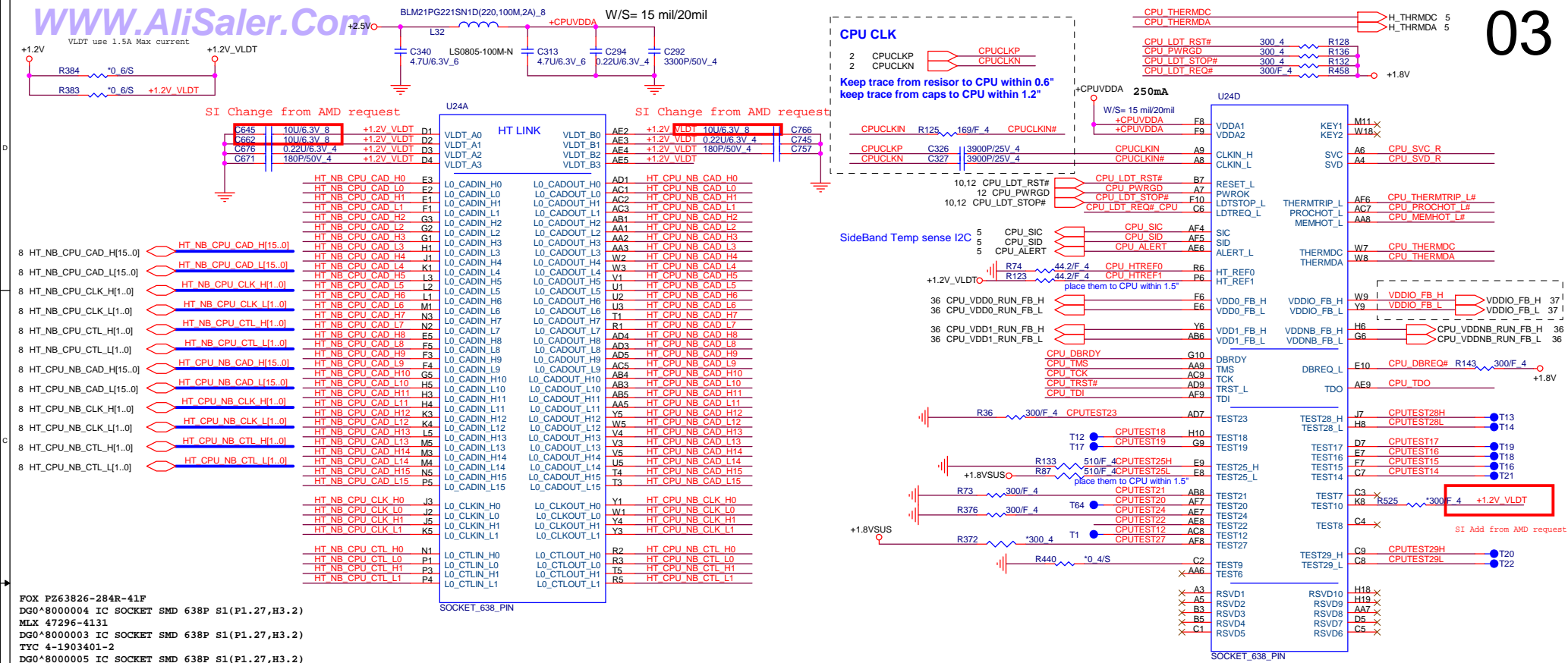


3

SLG8SP628VTR--AL8SP628000  
RTM880N-796-- AL000880001

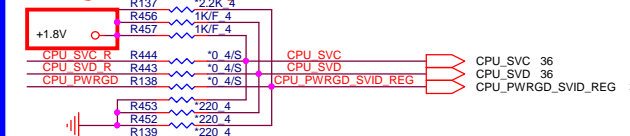
A

Size Custom	Document Number <b>Clock Generator</b>	Rev 1A
Date: Friday, March 20, 2009		Sheet 2 of 42



## Serial VID

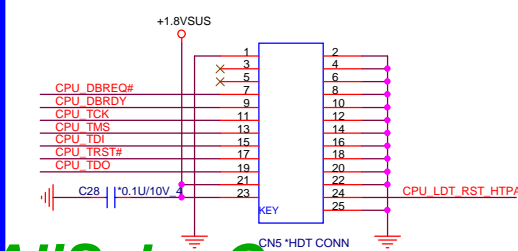
SI Change from AMD request



VFIX MODE VID Override Circuit

SVC	SVD	Voltage Output
0	0	1.4V
0	1	1.2V
1	0	1.0V
1	1	0.8V

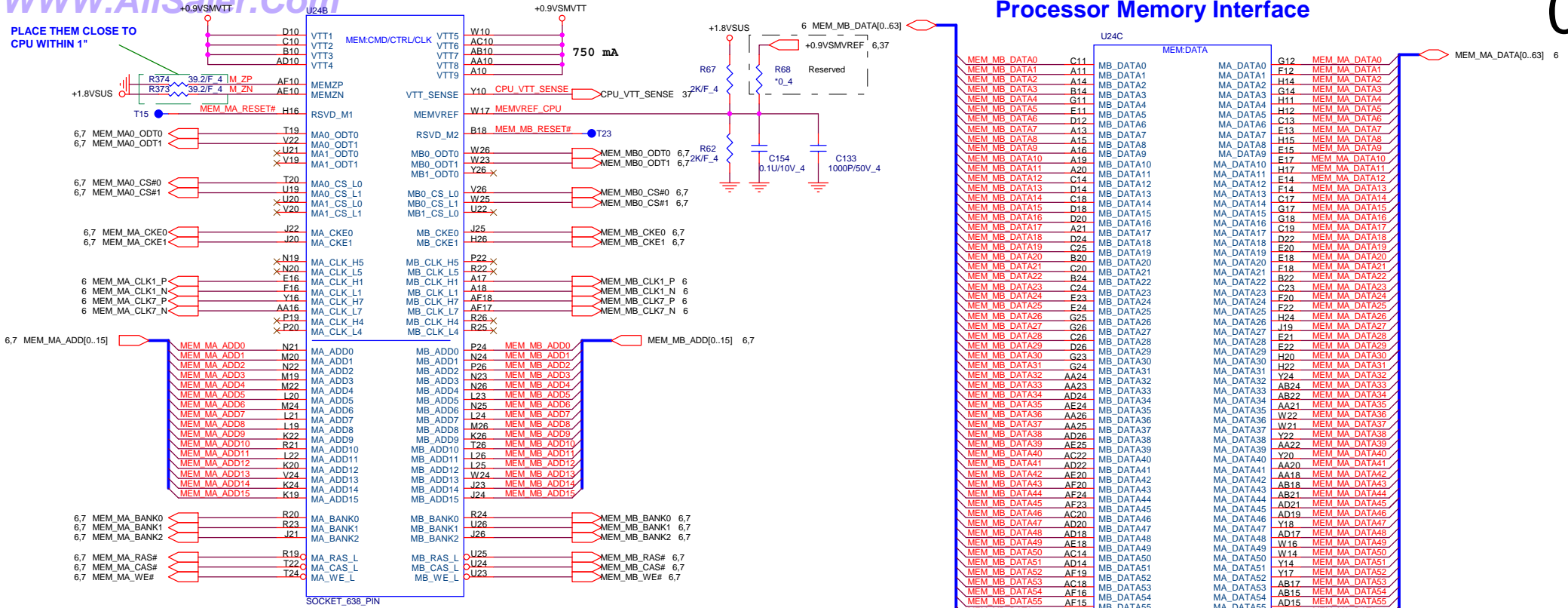
## HDT Connector



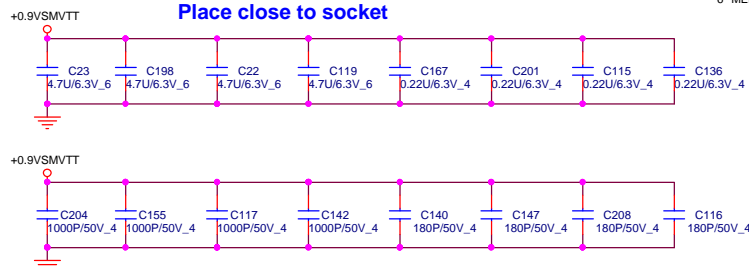
**PROJECT : OP8**  
 Quanta Computer Inc.

## Processor Memory Interface

PLACE THEM CLOSE TO CPU WITHIN 1"



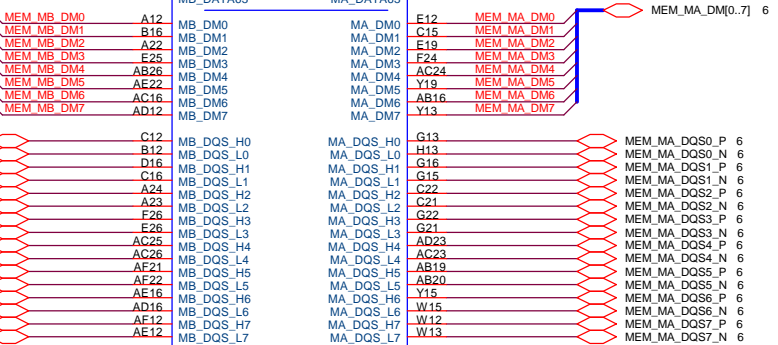
Place close to socket



Close to CPU within 1500 mils



PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH

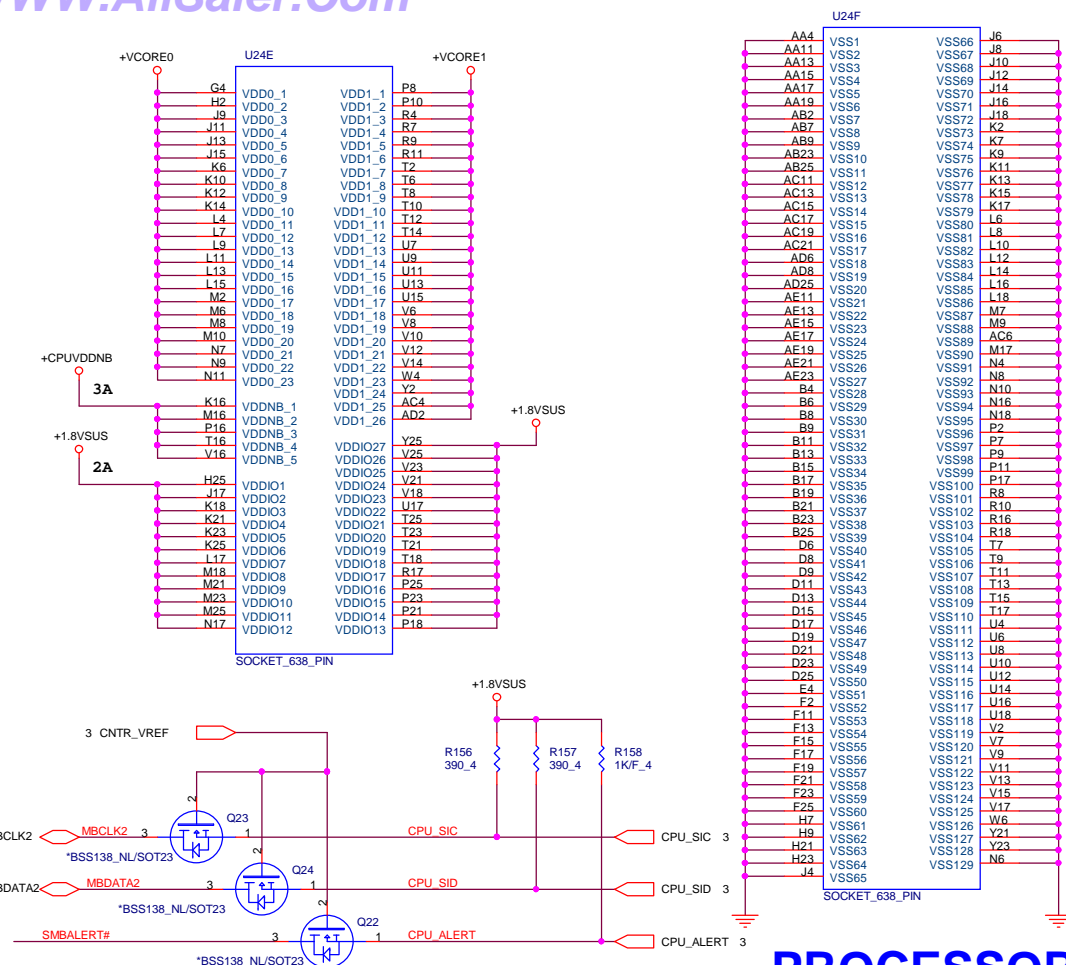


SOCKET\_638\_PIN

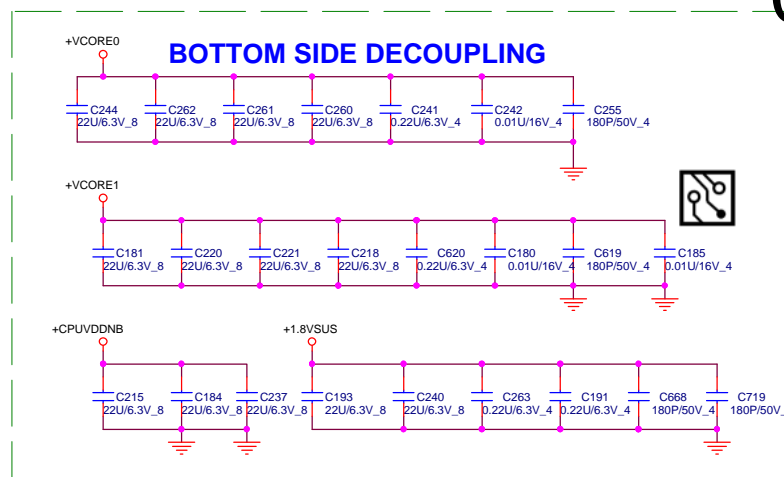


**PROJECT : OP8**  
Quanta Computer Inc.

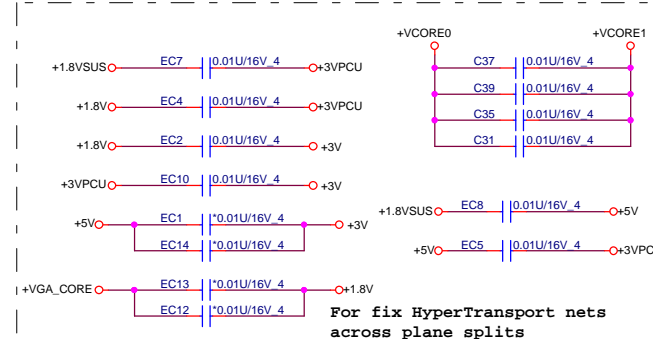
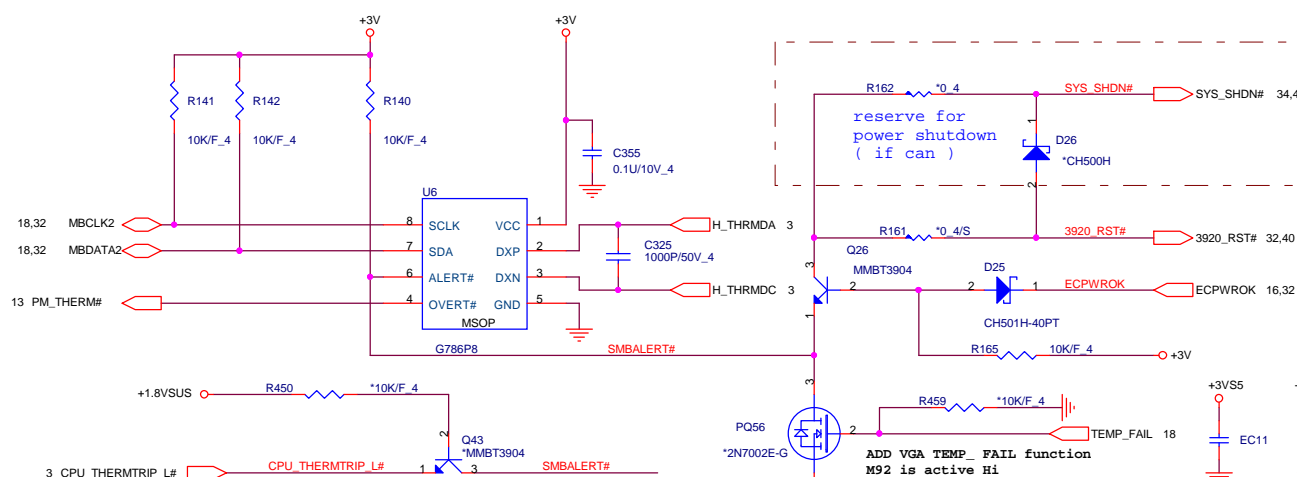
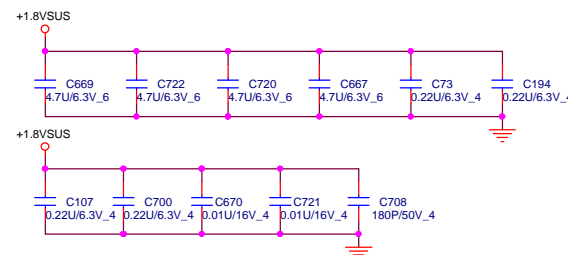
Size Custom Document Number S1G2 DDRII MEMORY I/F 2/3 Rev 1A  
Date: Friday, March 20, 2009 Sheet 4 of 42



## PROCESSOR POWER AND GROUND



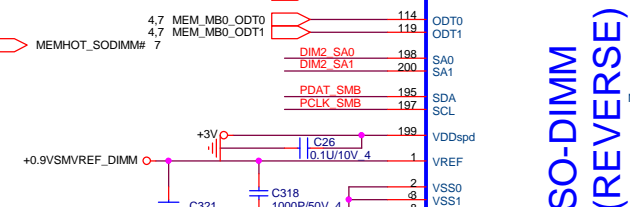
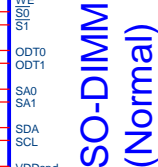
**DECOUPLING BETWEEN PROCESSOR AND DIMMs**  
**PLACE CLOSE TO PROCESSOR AS POSSIBLE**

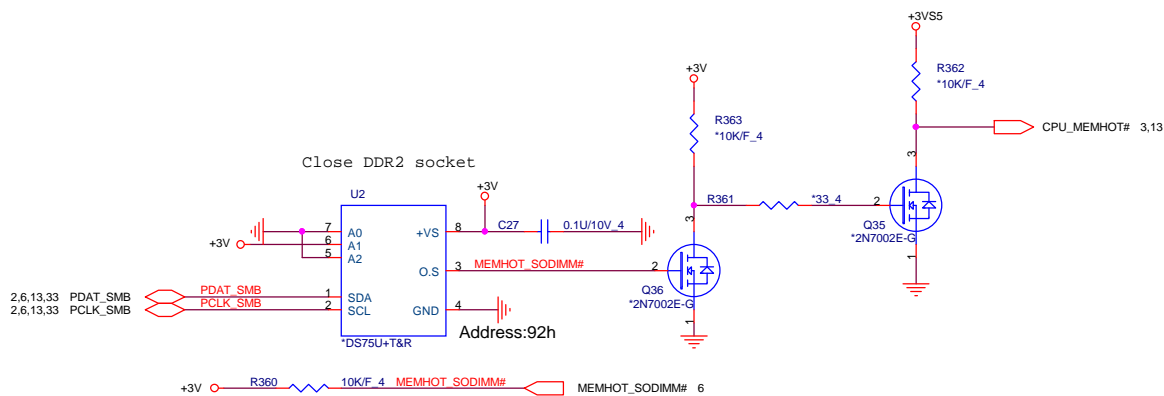
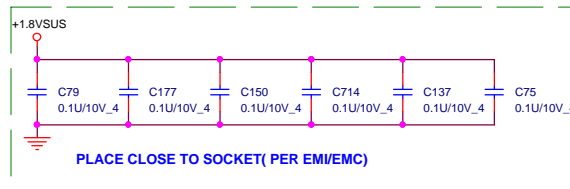
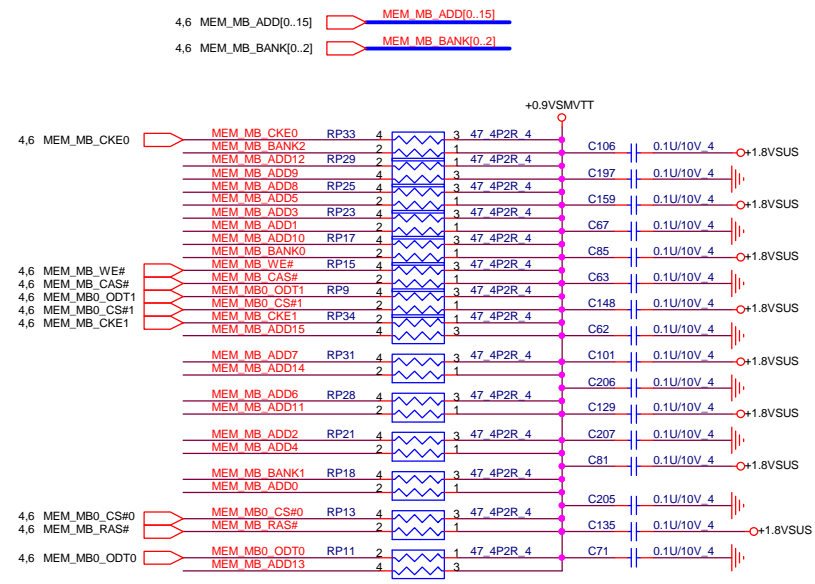
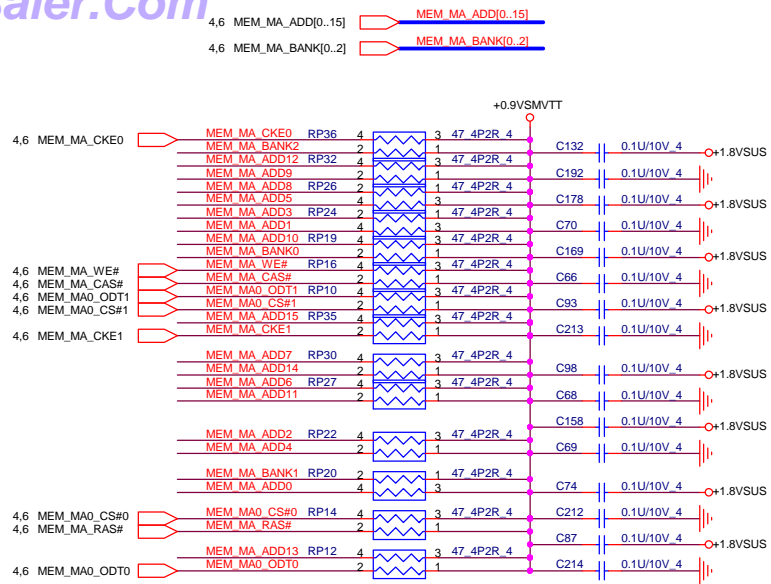


**PROJECT : OP8**  
Quanta Computer Inc.

Size Custom	Document Number <b>S1G2 PWR &amp; GND 3/3</b>	Rev 1/
Date: Friday, March 20, 2009		Sheet 5 of 42

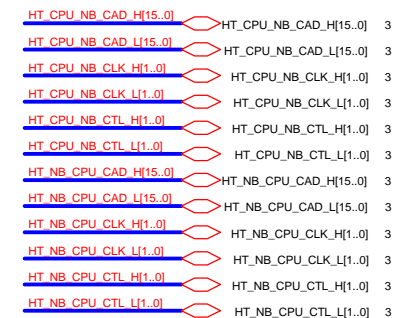






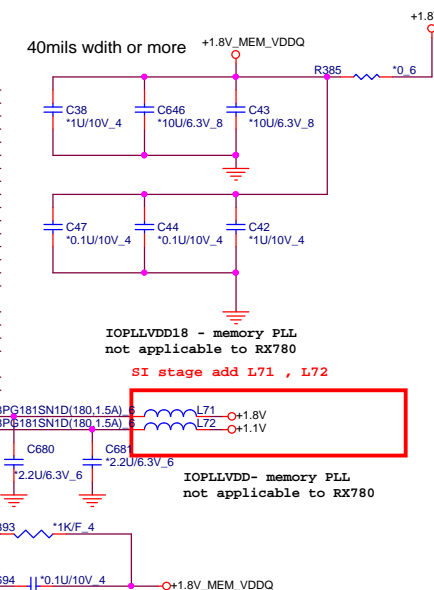
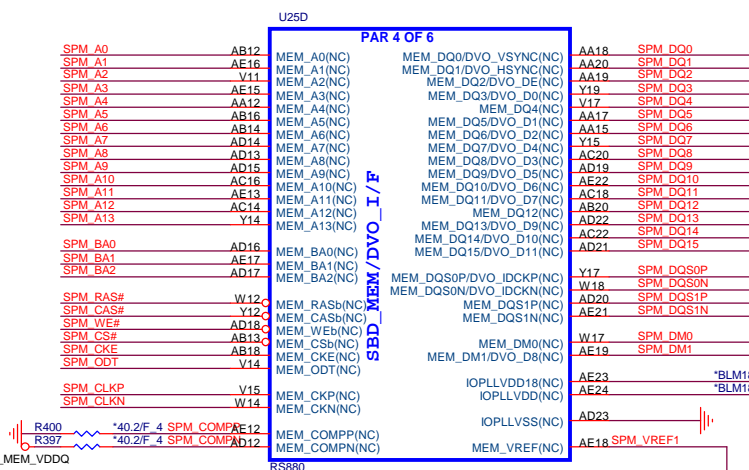
**PROJECT : OP8**  
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
DDR2 SODIMMS TERMINATIONS		
Date: Friday, March 20, 2009	Sheet 7	of 42



signals	RS880	RX880
HT_TXCALP	R430 301 ohm 1%	R430 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R434 301 ohm 1%	R434 1.21k ohm 1%
HT_RXCALN		

RES CHIP 301 1/16W +-1%(0402)  
P/N : CS13012FB14



IOPLLVD18 - memory PLL  
not applicable to RX780

SI stage add L71 , L72

IOPLLVD- memory PLL  
not applicable to RX780



**PROJECT : OP8**  
Quanta Computer Inc.

Size Custom	Document Number <b>RS740/RS780-HT LINK I/F 1/5</b>	Rev 1/A
Date: Friday, March 20, 2009	Sheet 8 of 42	



PART 2 OF 6

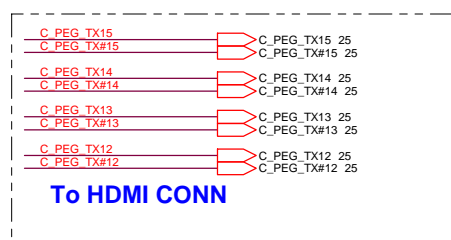
PCIE I/F GFX

PEG_RX15	D4	GFX_RX0P
PEG_RX#15	C4	GFX_RX0N
PEG_RX14	A3	GFX_RX1P
PEG_RX#14	B3	GFX_RX1N
PEG_RX13	C2	GFX_RX2P
PEG_RX#13	C1	GFX_RX2N
PEG_RX12	E5	GFX_RX3P
PEG_RX#12	F5	GFX_RX3N
PEG_RX11	G6	GFX_RX4P
PEG_RX#11	G6	GFX_RX4N
PEG_RX10	H6	GFX_RX5P
PEG_RX#10	H6	GFX_RX5N
PEG_RX9	J6	GFX_RX6P
PEG_RX#9	J5	GFX_RX6N
PEG_RX8	J7	GFX_RX7P
PEG_RX#8	J8	GFX_RX7N
PEG_RX7	L6	GFX_RX8P
PEG_RX#7	L6	GFX_RX8N
PEG_RX6	M8	GFX_RX9P
PEG_RX#6	L8	GFX_RX9N
PEG_RX5	P7	GFX_RX10P
PEG_RX#5	M7	GFX_RX10N
PEG_RX4	P5	GFX_RX11P
PEG_RX#4	P5	GFX_RX11N
PEG_RX3	R8	GFX_RX12P
PEG_RX#3	P8	GFX_RX12N
PEG_RX2	R6	GFX_RX13P
PEG_RX#2	R5	GFX_RX13N
PEG_RX1	P4	GFX_RX14P
PEG_RX#1	P3	GFX_RX14N
PEG_RX0	T4	GFX_RX15P
PEG_RX#0	T3	GFX_RX15N

A5	C	PEG_TX15	C332	0.1U/10V_4	PEG_TX15
B5	C	PEG_TX#15	C333	0.1U/10V_4	PEG_TX#15
A4	C	PEG_TX14	C339	0.1U/10V_4	PEG_TX14
B4	C	PEG_TX#14	C338	0.1U/10V_4	PEG_TX#14
C3	C	PEG_TX13	C336	0.1U/10V_4	PEG_TX13
B2	C	PEG_TX#13	C337	0.1U/10V_4	PEG_TX#13
D1	C	PEG_TX12	C335	0.1U/10V_4	PEG_TX12
D2	C	PEG_TX#12	C334	0.1U/10V_4	PEG_TX#12
E2	C	PEG_TX11	C735	0.1U/10V_4	PEG_TX11
E1	C	PEG_TX#11	C734	0.1U/10V_4	PEG_TX#11
F4	C	PEG_TX10	C729	0.1U/10V_4	PEG_TX10
F3	C	PEG_TX#10	C730	0.1U/10V_4	PEG_TX#10
F1	C	PEG_TX9	C727	0.1U/10V_4	PEG_TX9
F2	C	PEG_TX#9	C724	0.1U/10V_4	PEG_TX#9
H4	C	PEG_TX8	C726	0.1U/10V_4	PEG_TX8
H3	C	PEG_TX#8	C725	0.1U/10V_4	PEG_TX#8
H1	C	PEG_TX7	C723	0.1U/10V_4	PEG_TX7
H2	C	PEG_TX#7	C718	0.1U/10V_4	PEG_TX#7
J2	C	PEG_TX6	C716	0.1U/10V_4	PEG_TX6
J1	C	PEG_TX#6	C717	0.1U/10V_4	PEG_TX#6
K4	C	PEG_TX5	C710	0.1U/10V_4	PEG_TX5
K3	C	PEG_TX#5	C712	0.1U/10V_4	PEG_TX#5
K1	C	PEG_TX4	C713	0.1U/10V_4	PEG_TX4
K2	C	PEG_TX#4	C715	0.1U/10V_4	PEG_TX#4
M4	C	PEG_TX3	C707	0.1U/10V_4	PEG_TX3
M3	C	PEG_TX#3	C709	0.1U/10V_4	PEG_TX#3
M1	C	PEG_TX2	C706	0.1U/10V_4	PEG_TX2
M2	C	PEG_TX#2	C705	0.1U/10V_4	PEG_TX#2
N2	C	PEG_TX1	C703	0.1U/10V_4	PEG_TX1
N1	C	PEG_TX#1	C704	0.1U/10V_4	PEG_TX#1
P1	C	PEG_TX0	C699	0.1U/10V_4	PEG_TX0
P2	C	PEG_TX#0	C701	0.1U/10V_4	PEG_TX#0



Close to North Bridge



To HDMI CONN

PCIE I/F GPP

33	PCIE_RXP1	AE3	GPP_RX0P
33	PCIE_RXN1	AD4	GPP_RX0N
30	PCIE_RXP2_LAN	AE2	GPP_RX1P
30	PCIE_RXN2_LAN	AD3	GPP_RX1N
		AD1	GPP_RX2P
		AD2	GPP_RX2N
		V5	GPP_RX3P
		W6	GPP_RX3N
		U5	GPP_RX4P
		U6	GPP_RX4N
		U8	GPP_RX5P
		U7	GPP_RX5N

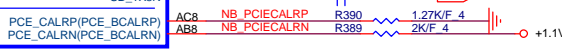
AC1	X	GPP_TX0P
AC2	X	GPP_TX0N
AB3	C	PCIE_TXP1 C C88
AB4	C	PCIE_TXN1 C C89
AA2	C	PCIE_TXP2 C C679
AA1	C	PCIE_TXN2 C C696
Y1	X	GPP_TX3P
Y2	X	GPP_TX3N
Y3	X	GPP_TX4P
Y4	X	GPP_TX4N
V1	X	GPP_TX5P
V2	X	GPP_TX5N

TO WLAN  
TO PCIE-LAN

PCIE I/F SB

12	PCIE_SB_NB_RX0P	AA8	SB_RX0P
12	PCIE_SB_NB_RX0N	Y8	SB_RX0N
12	PCIE_SB_NB_RX1P	AA7	SB_RX1P
12	PCIE_SB_NB_RX1N	Y7	SB_RX1N
12	PCIE_SB_NB_RX2P	AA5	SB_RX2P
12	PCIE_SB_NB_RX2N	AA6	SB_RX2N
12	PCIE_SB_NB_RX3P	W5	SB_RX3P
12	PCIE_SB_NB_RX3N	Y5	SB_RX3N

AD7	A	TX0P C C686	0.1U/10V_4	PCIE_NB_SB_TX0P	12
AE7	A	TX0N C C687	0.1U/10V_4	PCIE_NB_SB_TX0N	12
AE6	A	TX1P C C685	0.1U/10V_4	PCIE_NB_SB_TX1P	12
AD6	A	TX1N C C684	0.1U/10V_4	PCIE_NB_SB_TX1N	12
AB6	A	TX2P C C690	0.1U/10V_4	PCIE_NB_SB_TX2P	12
AC6	A	TX2N C C691	0.1U/10V_4	PCIE_NB_SB_TX2N	12
AD5	A	TX3P C C688	0.1U/10V_4	PCIE_NB_SB_TX3P	12
AE5	A	TX3N C C689	0.1U/10V_4	PCIE_NB_SB_TX3N	12



RS880

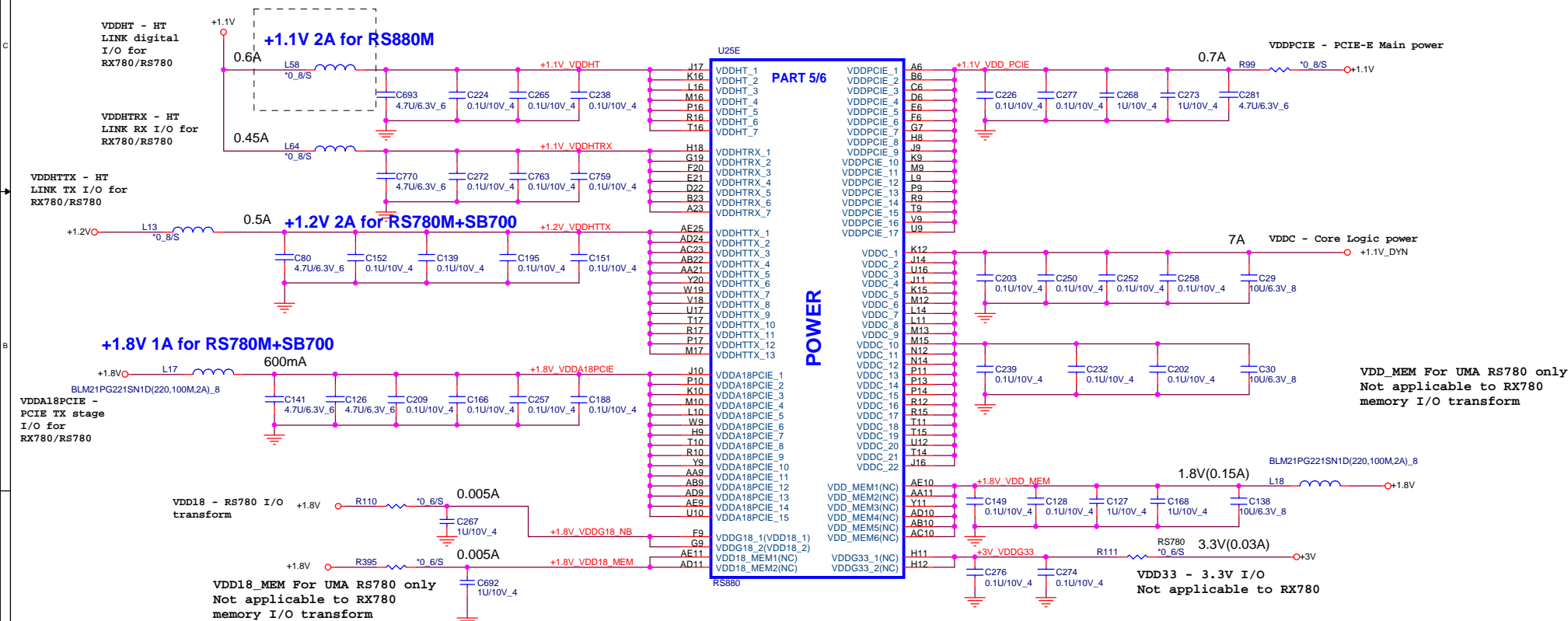
RS880 Display Port Support (muxed on GFX)

DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1

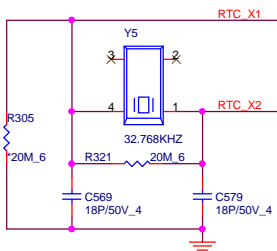




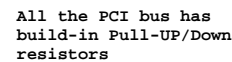
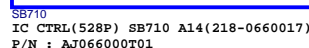
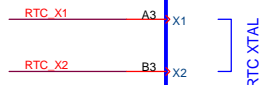
PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVDD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDL18	NC	+1.8V
IOPLLVDD18	NC	+1.8V	VDDL18T33	NC	NC



To RS780



FOR A14 chip



```
INTRUDER_ALERT# Left not connected (Southbridge
has 50-kohm internal pull-up to VBAT).
```



Rev	1/
-----	----

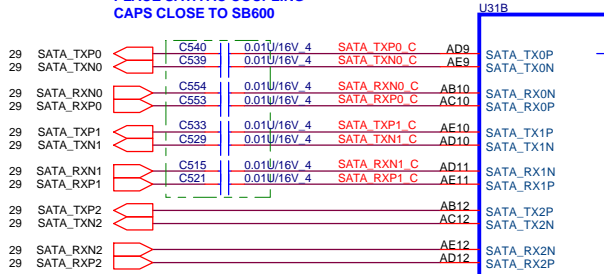




SATA1

SATA ODD

E-SATA



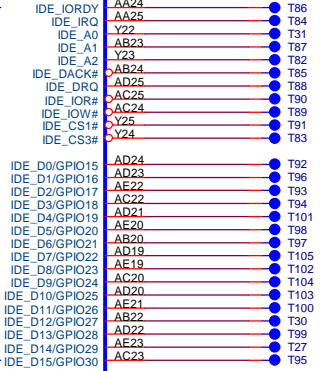
SB710  
Part 2 of 5

SERIAL ATA

ATA 66/100/133

SATA PWR

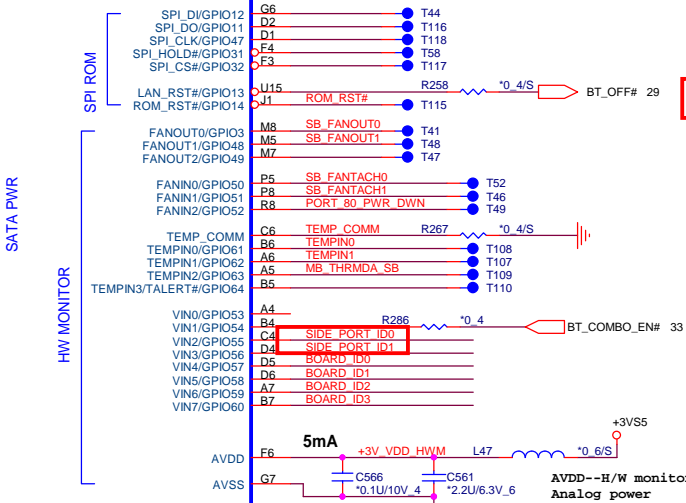
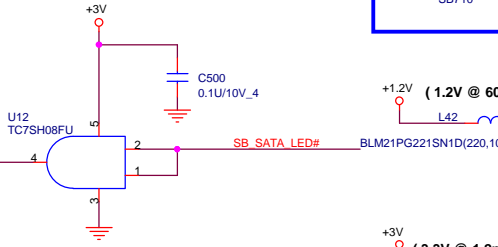
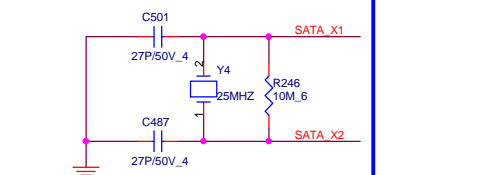
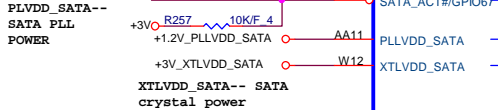
HW MONITOR



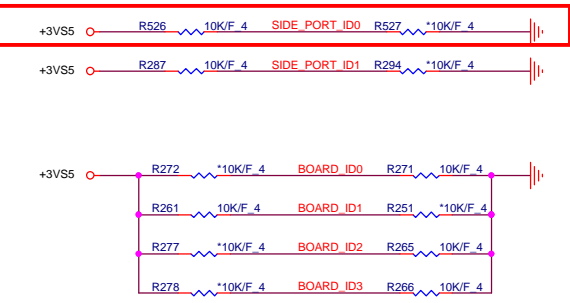
IF THERE IS NO IDE, TEST  
POINTS FOR DEBUG BUS  
IS MANDATORY

SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	Samsung
0	1	Qimonda
1	0	Hynix
1	1	no support side port

NOTE:  
R361 IS 1K 1% FOR 25MHz  
XTAL, 4.99K 1% FOR 100MHz  
INTERNAL CLOCK



Add for design

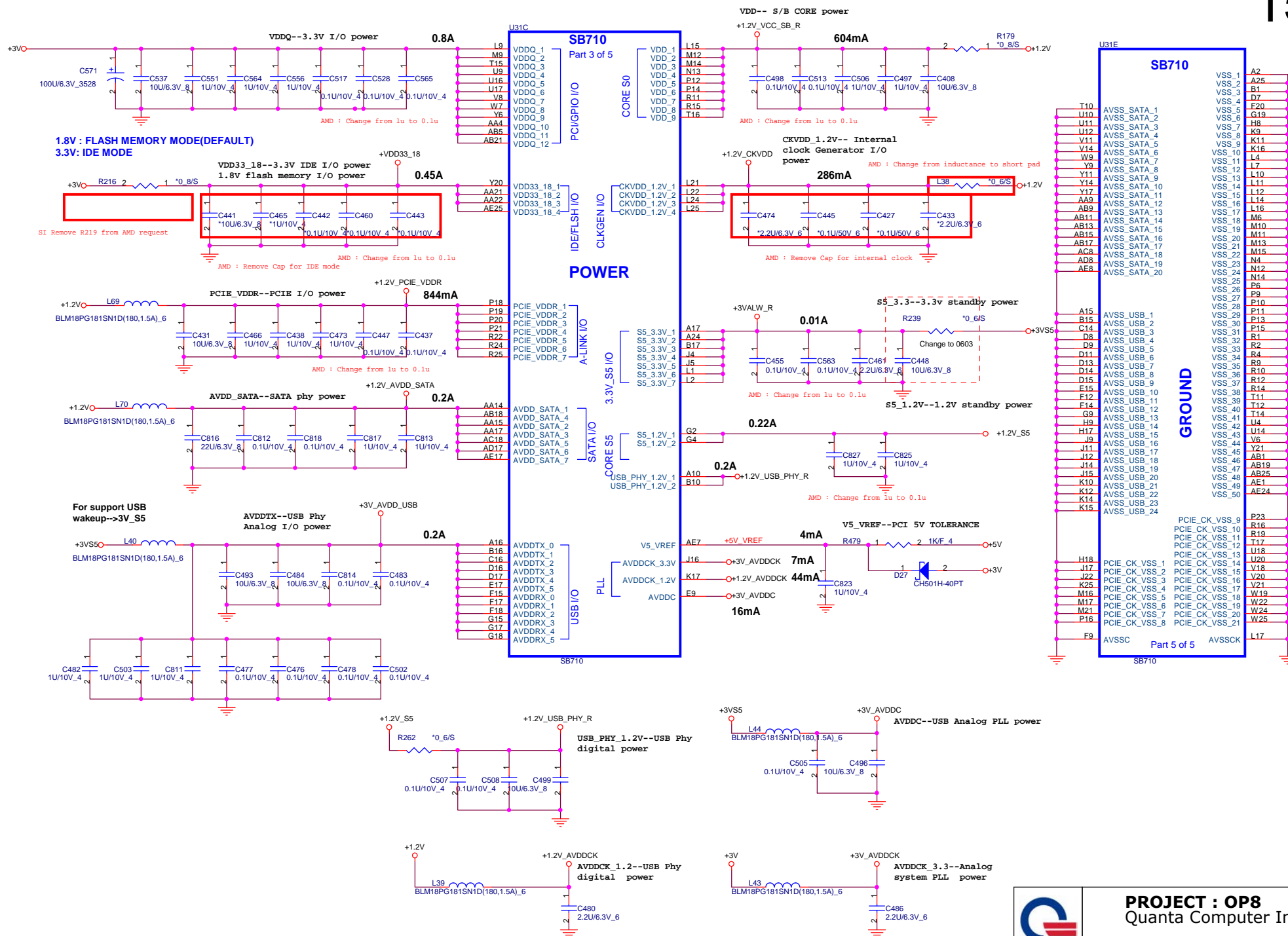


ID3	ID2	ID1	ID0	
0	0	0	0	OP8 UMA
0	0	0	1	OP9 UMA
0	0	1	0	OP8 Dis
0	0	1	1	OP9 Dis
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	



PROJECT : OP8  
Quanta Computer Inc.

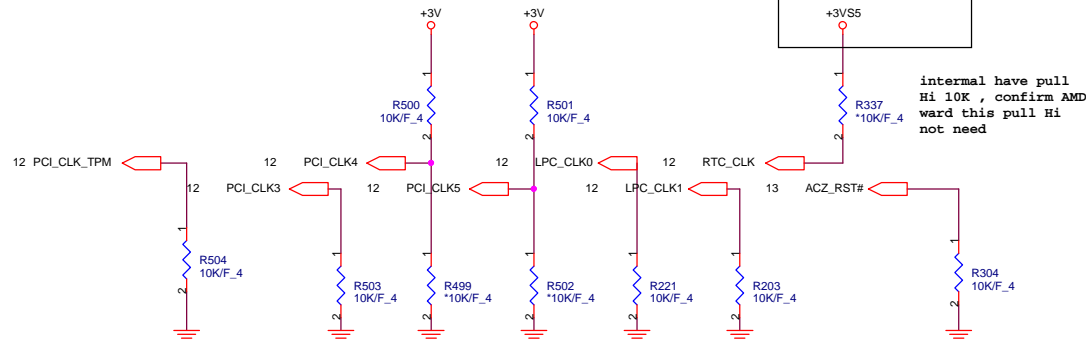
Size Custom Document Number SB700-ACPI/GPIO/USB 2/4 Rev 1A  
Date: Friday, March 20, 2009 Sheet 14 of 42



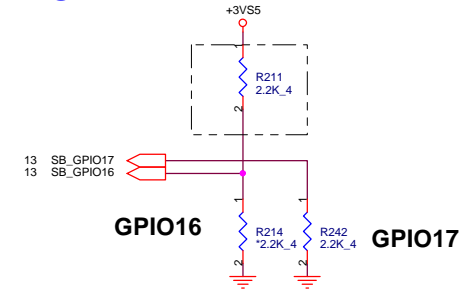


It must ready  
refoe RSMRST#

## REQUIRED STRAPS



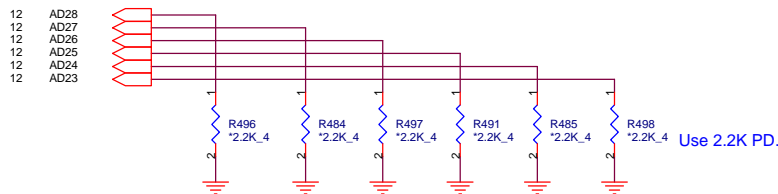
	PCI_CLK_TPM	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	IMC ENABLED	CLKGEN ENABLED	INTERNAL RTC  DEFAULT	ENABLE PCI ROM BOOT
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT



TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

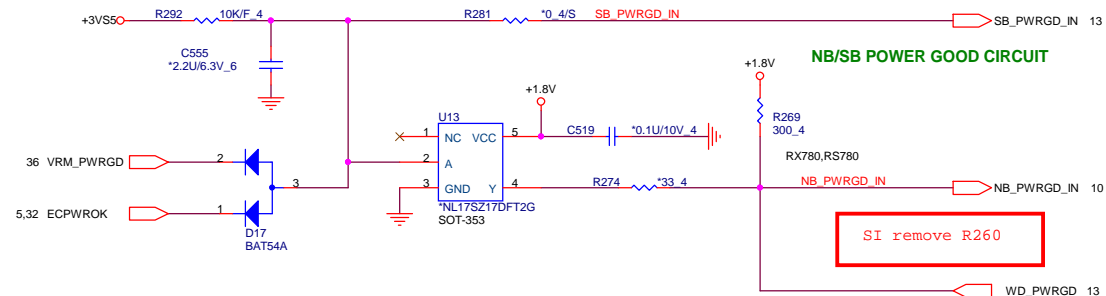
## DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI\_AD[28:23]



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB\_PWRGD\_IN:  
RS780/RX780 = 1.8V; RS740 = 3.3V  
Do NOT share it with SB\_PWRGD when use Internal Clk Gen  
(Need SB PLL initialize firstly)

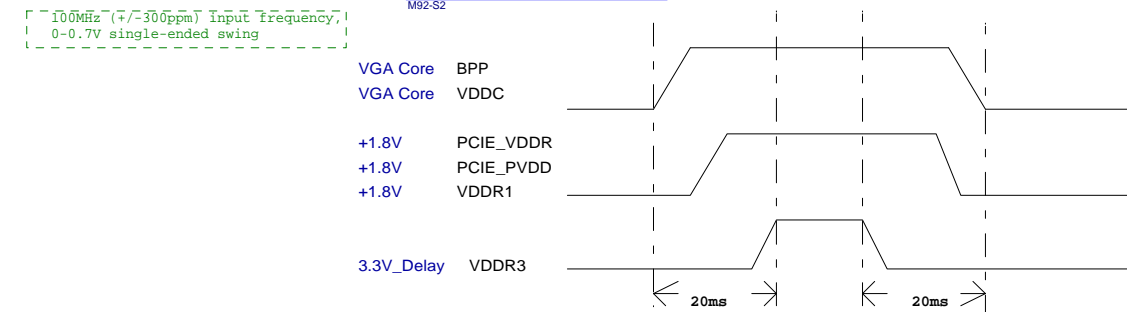
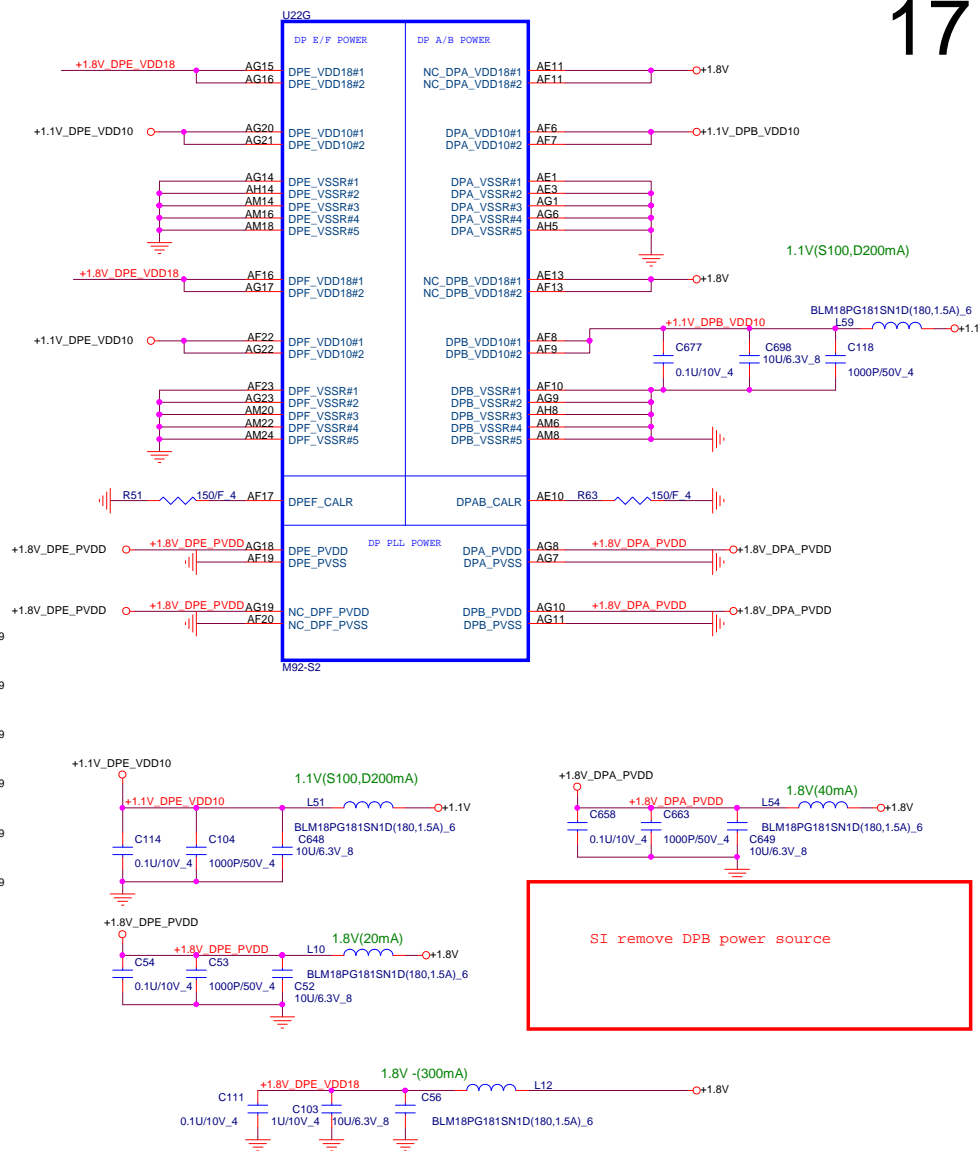


AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353  
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5



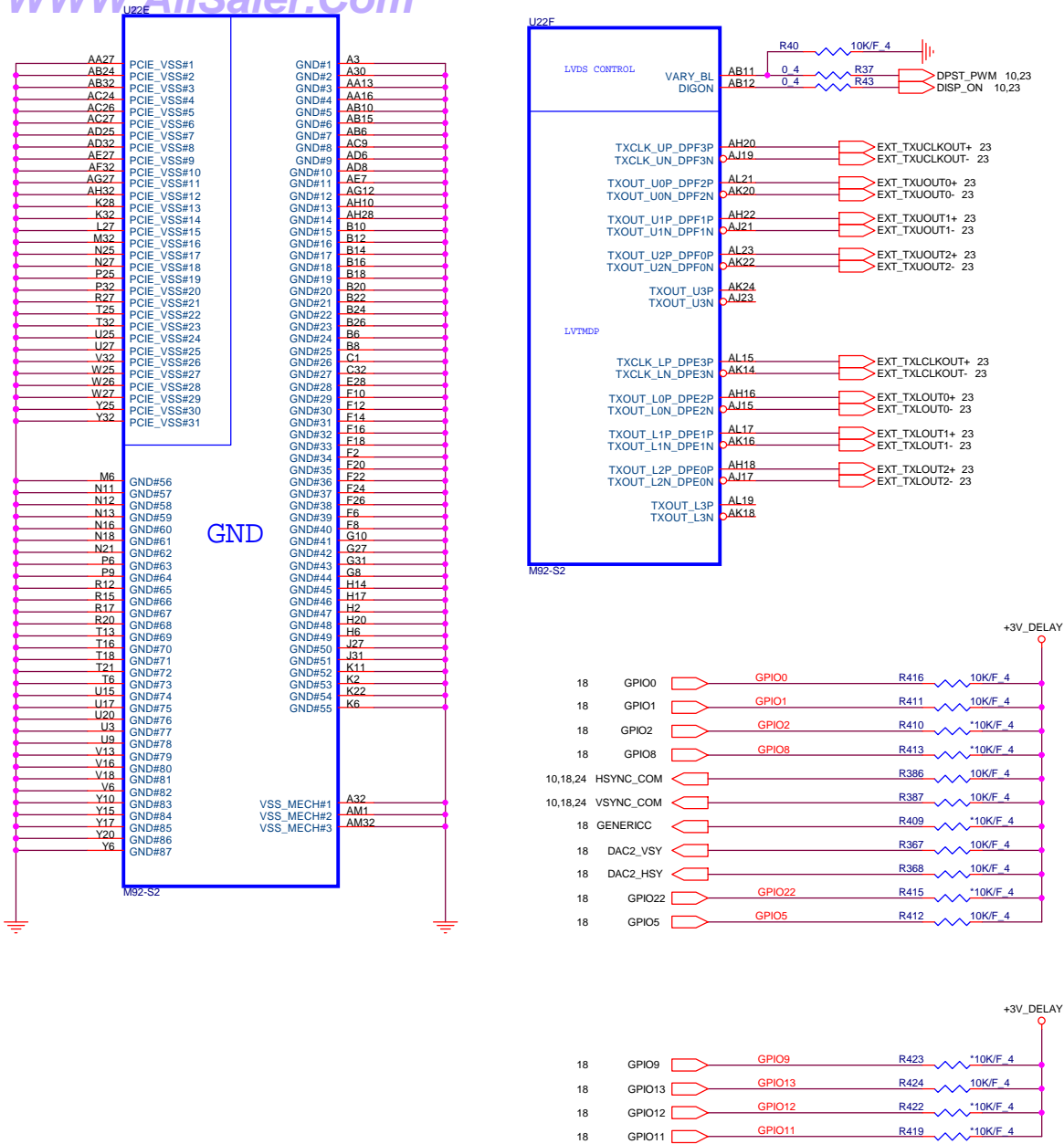
PROJECT : OP8  
Quanta Computer Inc.

Size Custom Document Number SB700-STRAPS Rev 1A  
Date: Friday, March 20, 2009 Sheet 16 of 42









Strap Name		Pin Straps description	Default Value
TX_PWRS_ENB	GPIO0	<b>Transmitter Power Savings Enable</b> 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	<b>PCI Express Transmitter De-emphasis Enable</b> 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	0
STRAP_BIF_CLK_PM_EN	GPIO8	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0
AUDIO[0]	VSYN		1
AUD(1)	HSYN	HSYN - HDMI_EN HDMI connector presence. 0 ?No HDMI connector is present on PCB 1 - HDMI connector is present on the PCB HDMI	1
VIP_DEVICE_STRAP_DIS	DAC2_VSY	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0
SMS_EN_HARD	DAC2_HSY		0
CCBYPASS	GENERIC		0

### Memory Aperture size

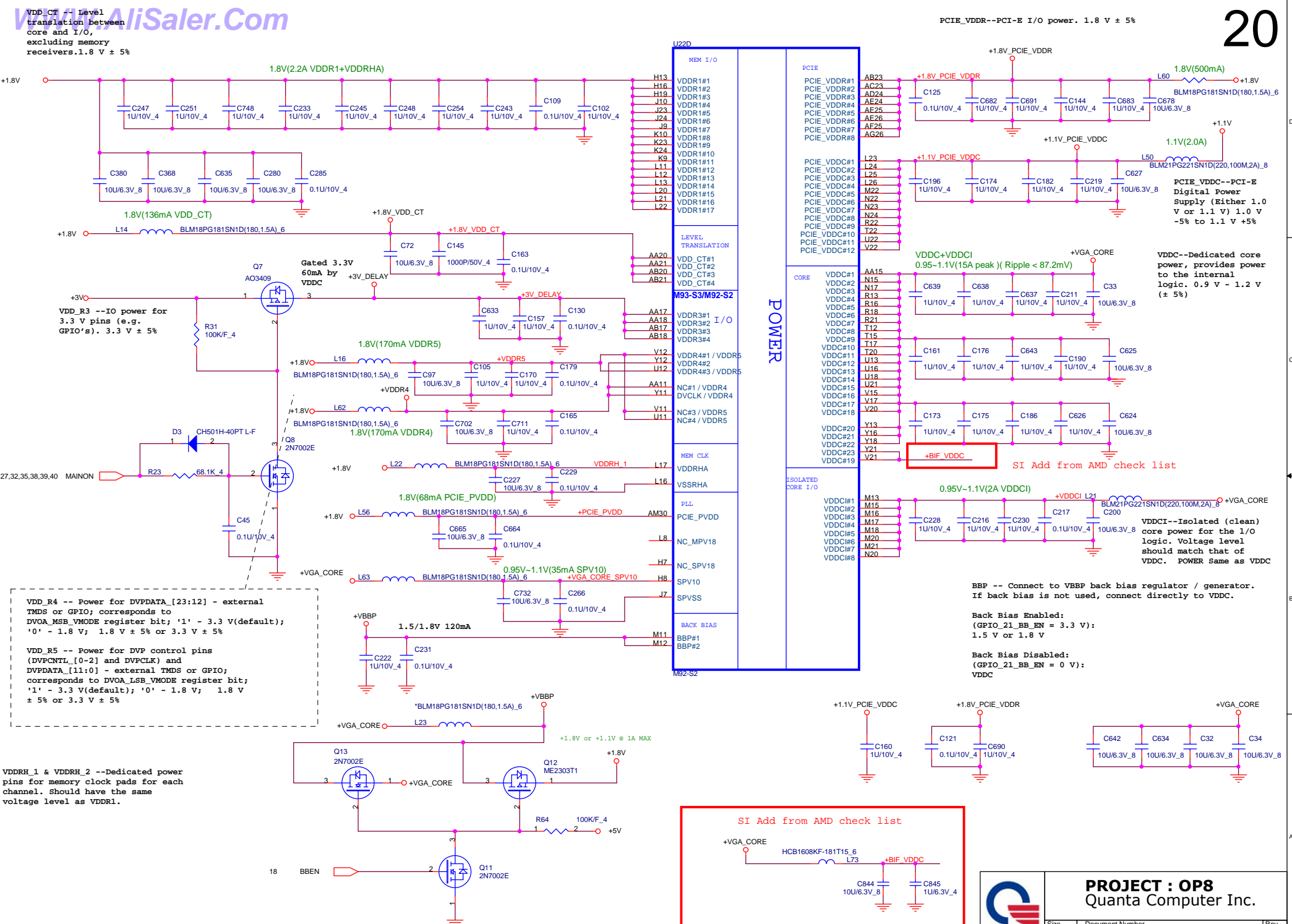
GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

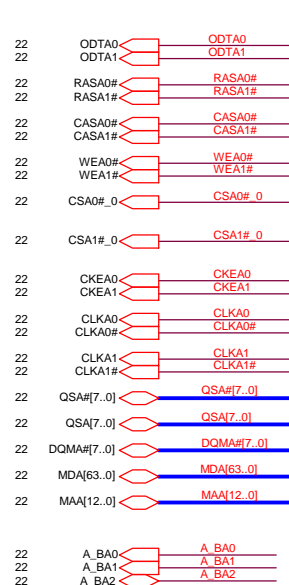
It is a shared pin strap with CONFIG[2:0] if BIOS\_ROM\_EN is set to 0.



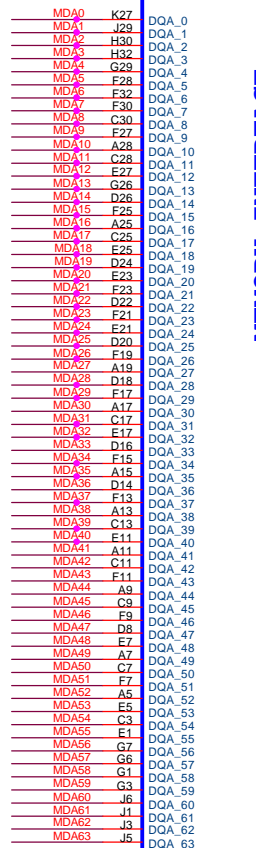
**PROJECT : OP8**  
Quanta Computer Inc.

Size Custom	Document Number <b>M7X/M8X_GND / LVDS/ Straps</b>	Rev 1A
Date: Friday, March 20, 2009		Sheet 19 of 42

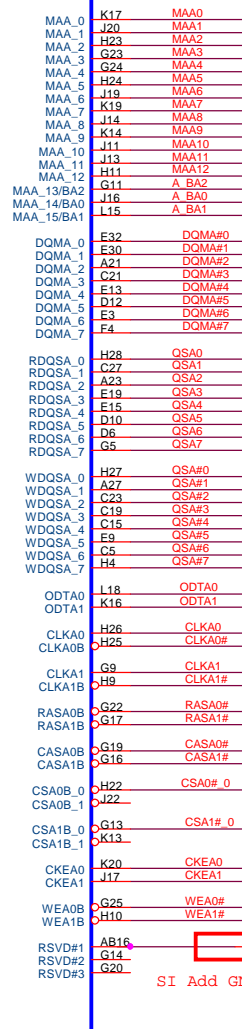




support 1Gbit  
VRAM ( 64M x 16 )



## MEMORY INTERFACE



SI Add GND from Check list

SI Add GND from Check list

Change MEMTEST to 240 1%  
ohm to GND , AMD update

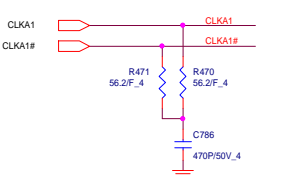
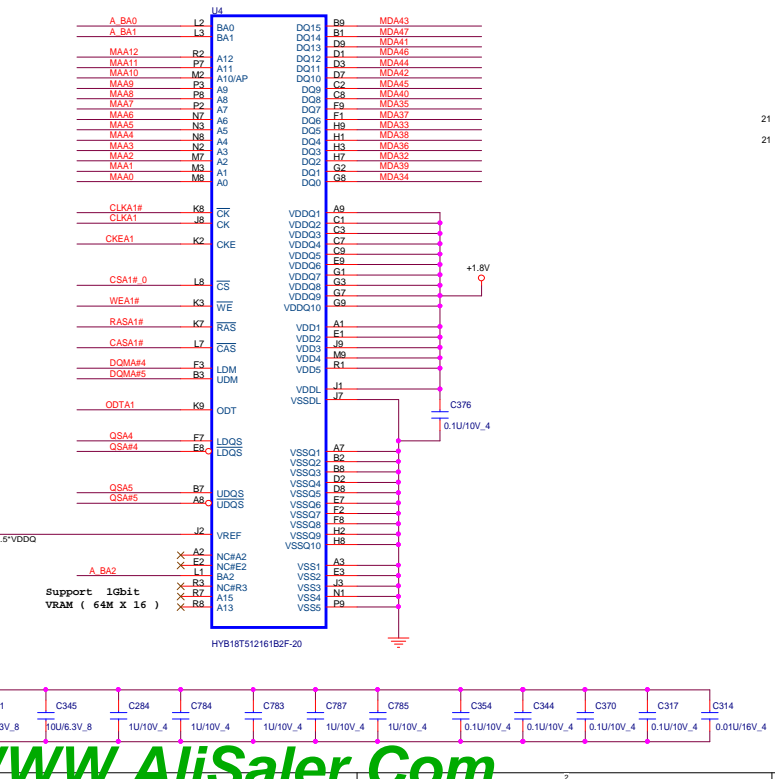
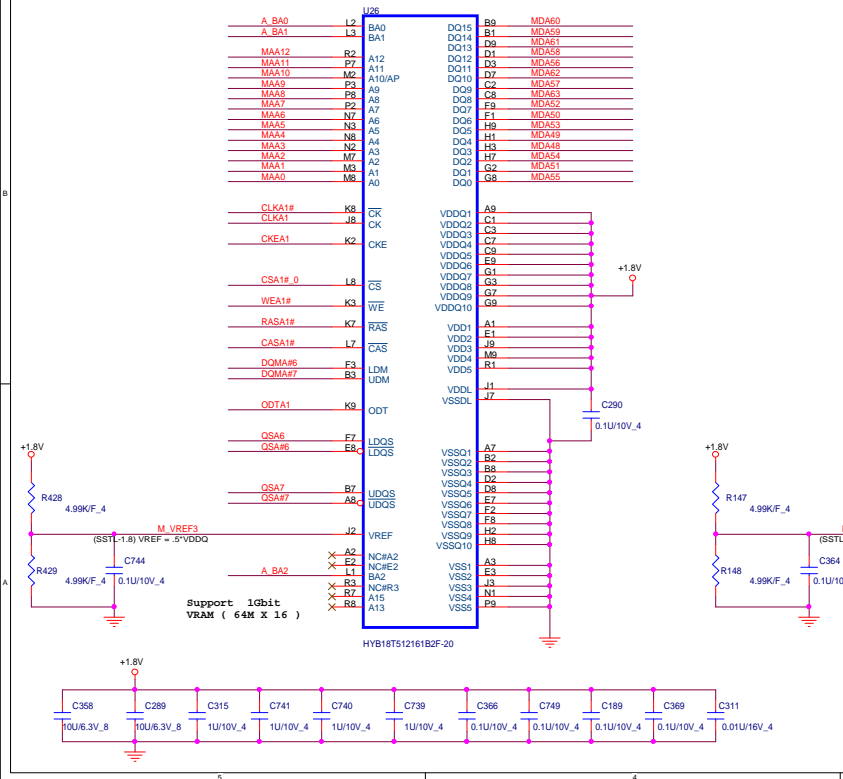
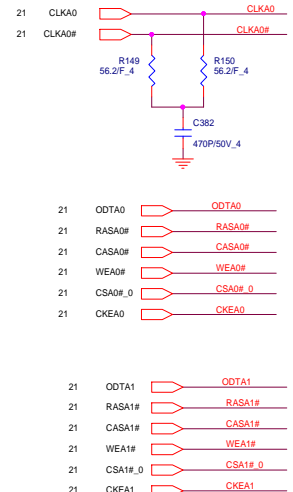
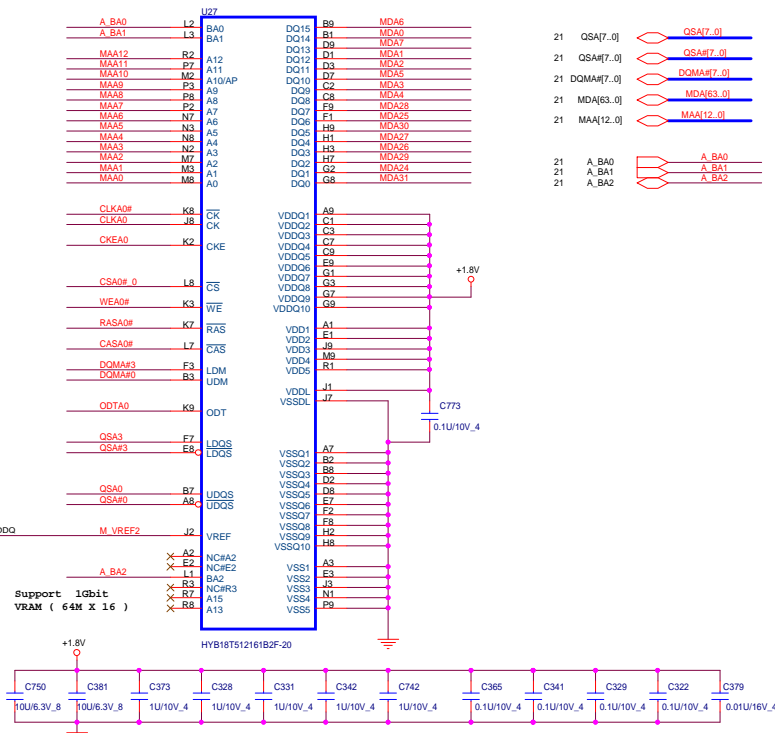
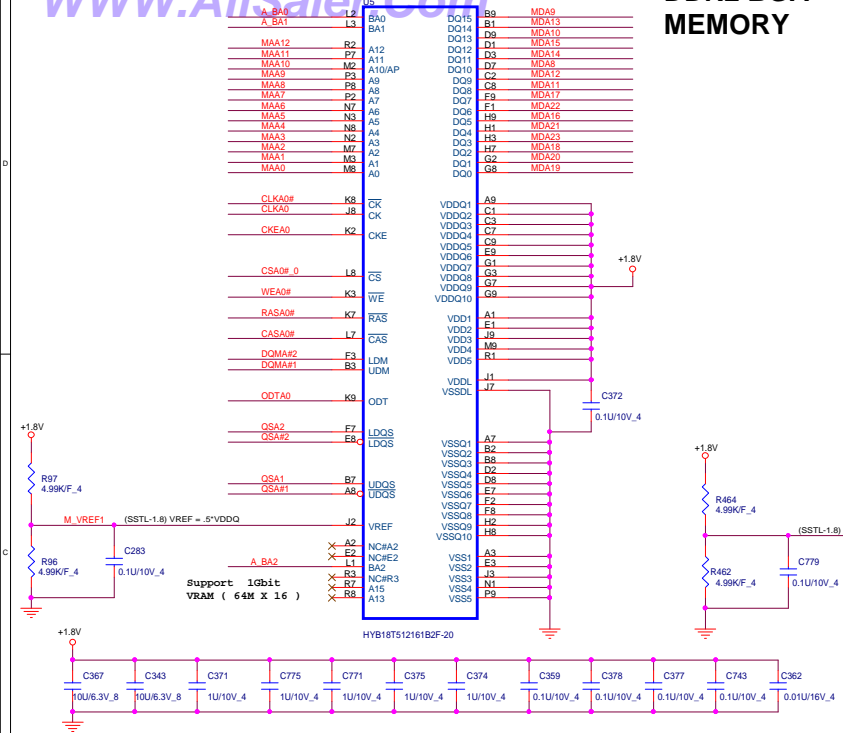


**PROJECT : OP8**  
Quanta Computer Inc.

Size Custom	Document Number <b>M7X/M8X/MEM_Interface</b>	Rev 1A
Date: Friday, March 20, 2009	Sheet 21 of 42	

# DDR2 BGA MEMORY

22



DDR2 BGA MEMORY

**PROJECT : OP8**  
Quanta Computer Inc.

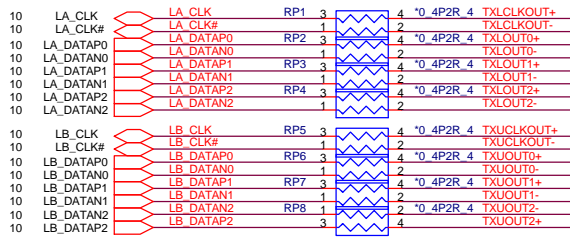
Size C Document Number  
**M92VRAM\_A0,A1**

Rev 1A

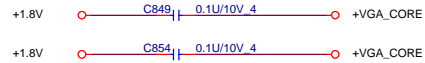
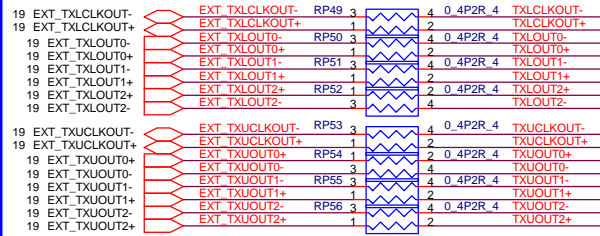
Date: Friday, March 20, 2009 Sheet 22 of 42

1. If LCD connector near GPU, then place these series Resistors near GPU  
2. If LCD connector near N/B, then place these series Resistors near N/B

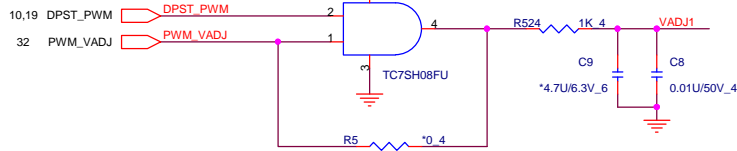
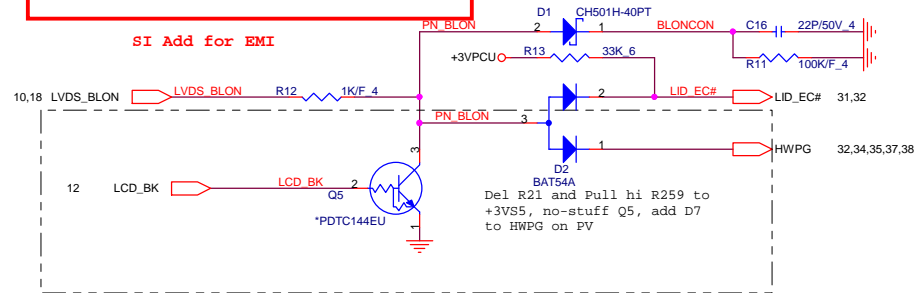
#### OPTION SIGNAL FROM NB to LVDS for UMA



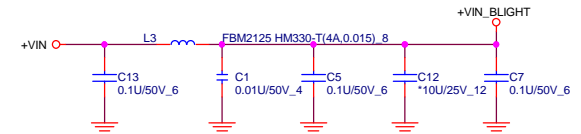
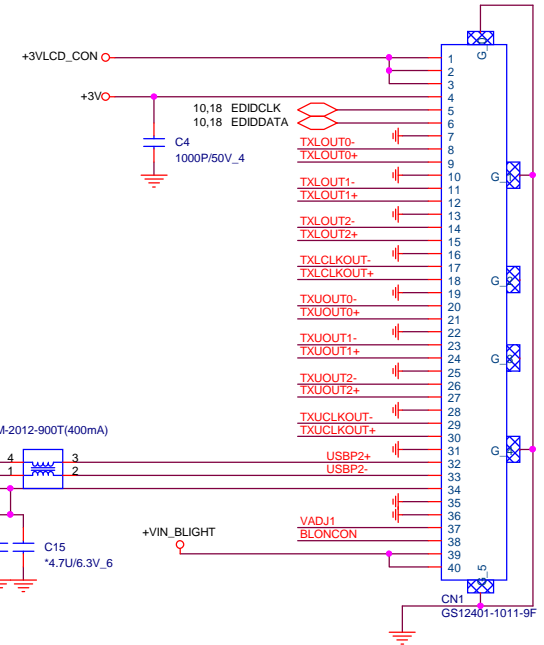
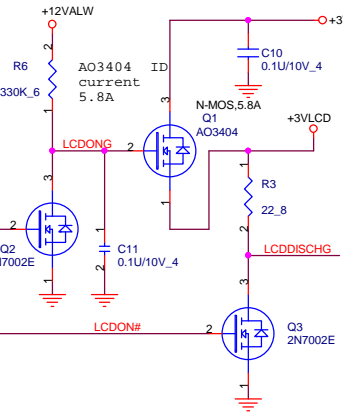
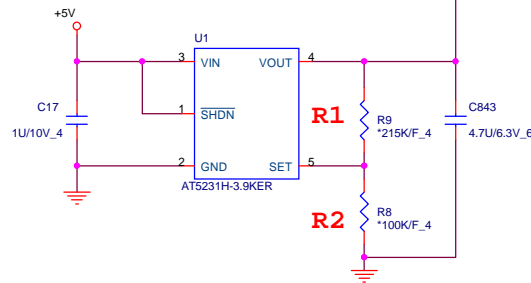
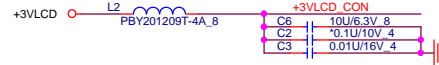
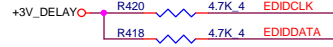
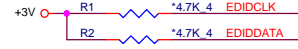
#### OPTION SIGNAL FROM M92 to LVDS for discrete



#### SI Add for EMI



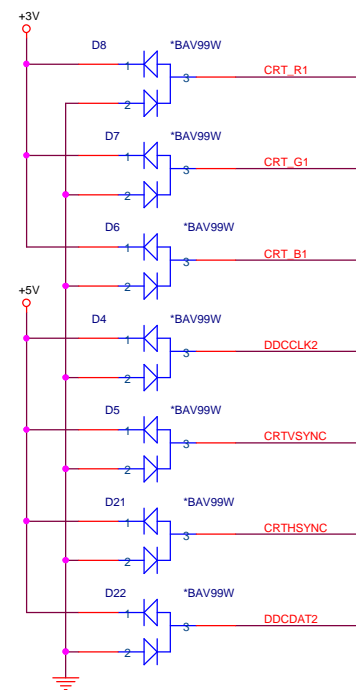
SI add U33,R524,C842 for Vari bright function



**PROJECT : OP8**  
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
	<b>LCD CONN</b>	
Date: Friday, March 20, 2009	Sheet 23 of 42	



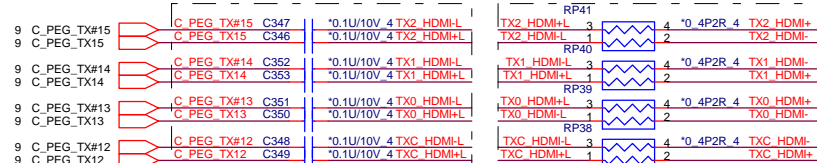


## UMA/DISCRETE select for HDMI

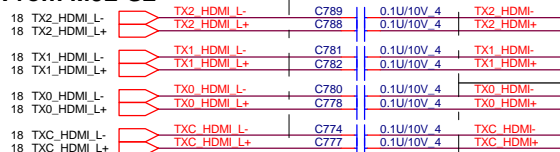
### From RS780M

for Layout  
concern  
,placement close  
north bridge

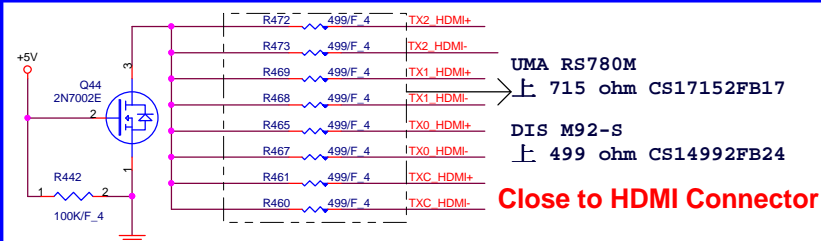
for Layout  
concern  
,placement close  
HDMI conn



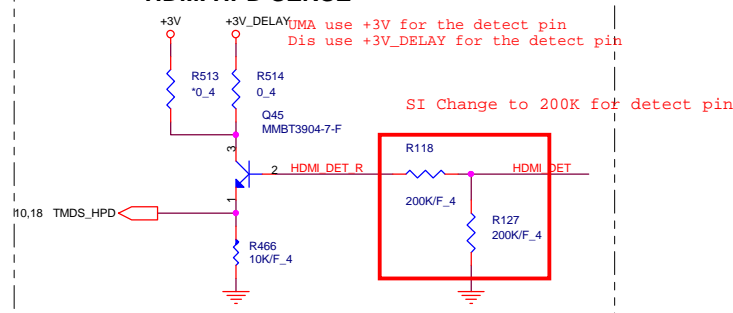
### From M92-S2



for Layout  
concern  
,placement close  
HDMI conn

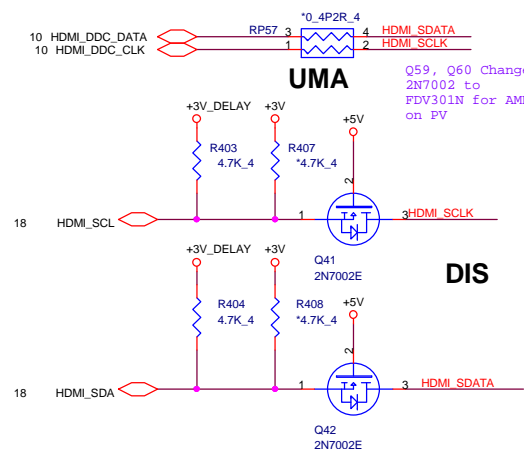


## HDMI HPD SENSE



## UMA AND DISCRETE HDMI I2C SELECT

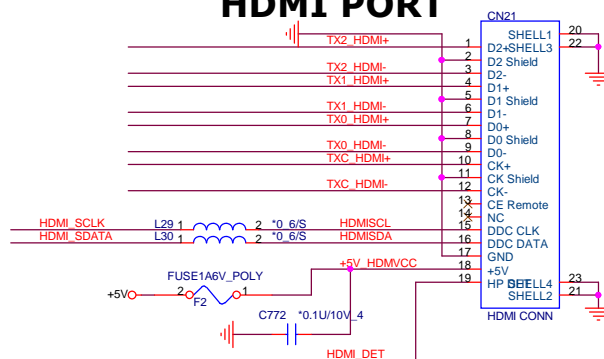
### Close to HDMI Connector



Discrete DDC4 is 5V  
tolerance , the MOSFET  
level shifter no need  
UMA DDC is 3V  
tolerance,the MOSFET  
level shifter is need

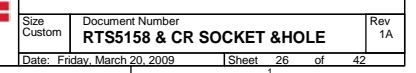
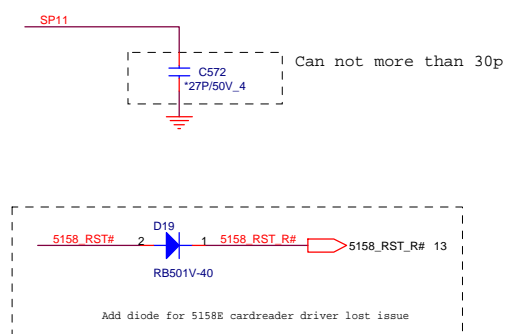
SI Change for DIS HDMI

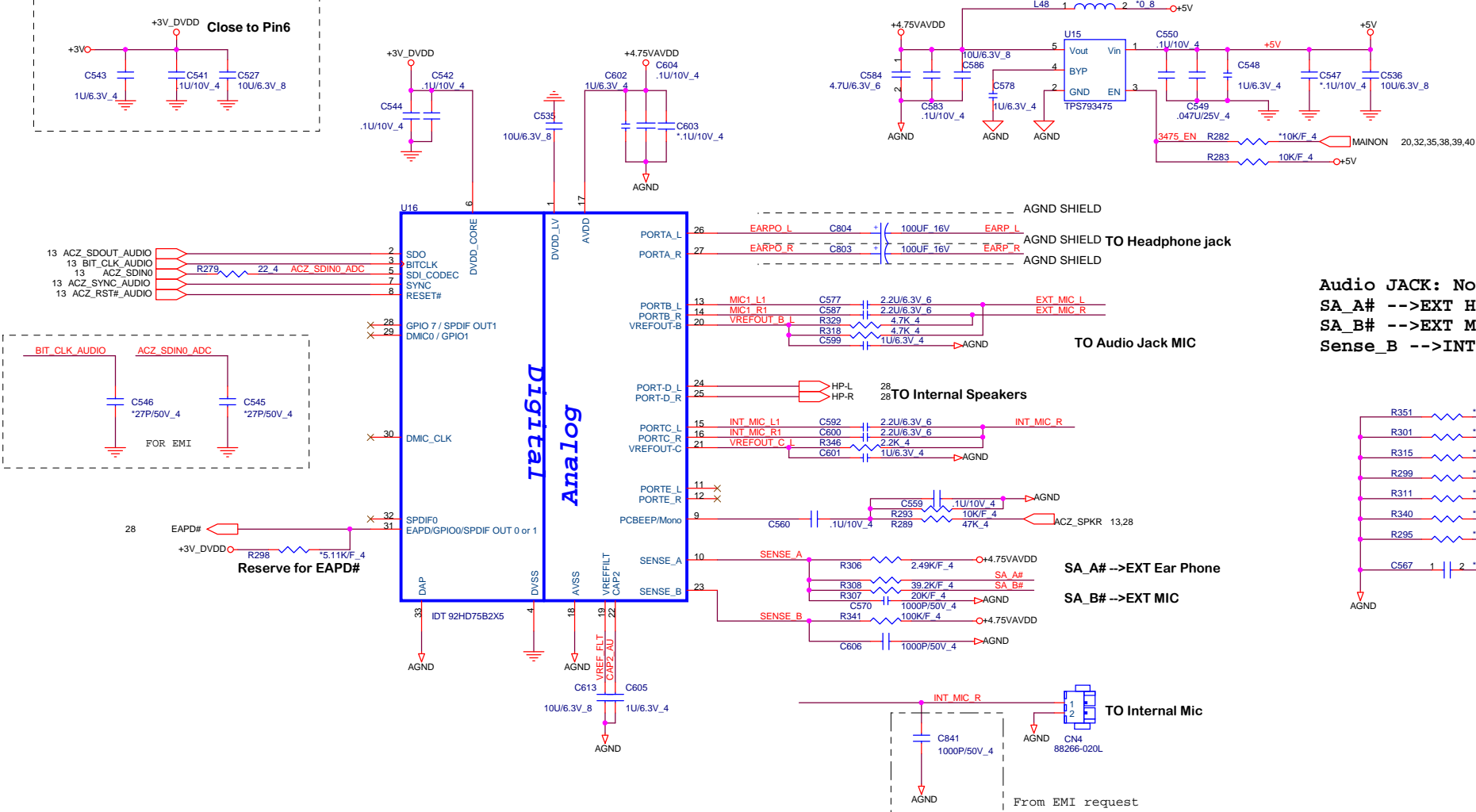
## HDMI PORT



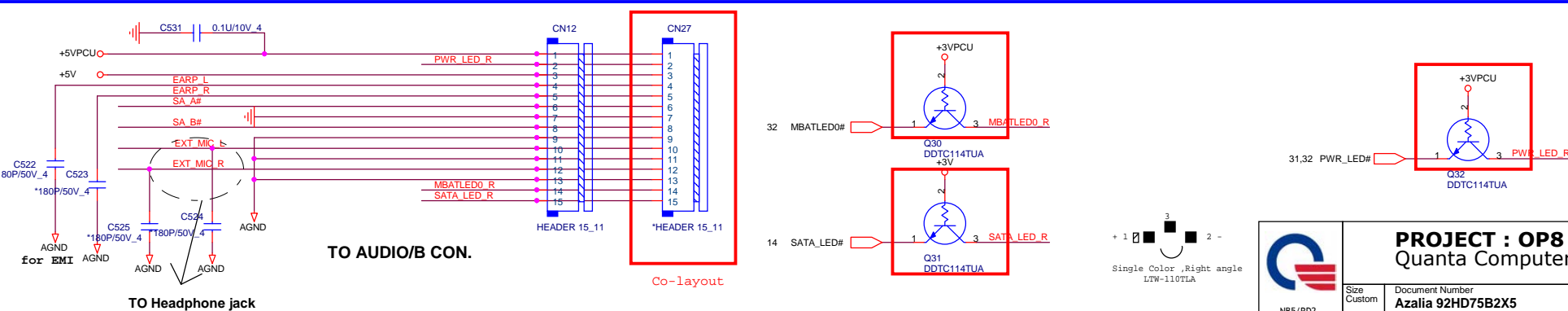
PROJECT : OP8  
Quanta Computer Inc.

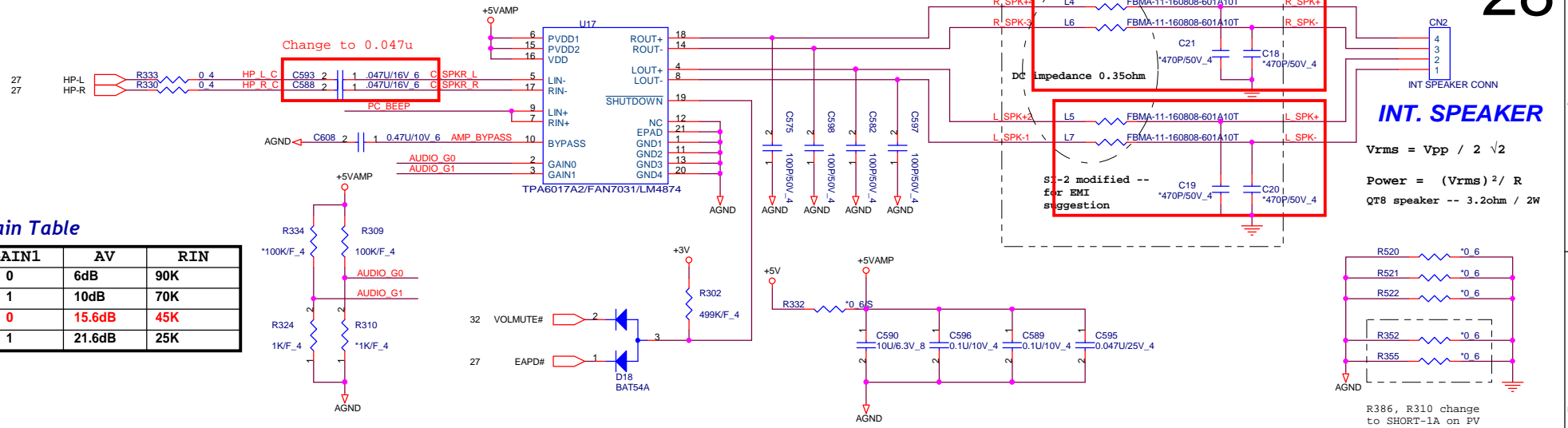
Size Custom	Document Number HDMI	Rev 1A
Date: Friday, March 20, 2009	Sheet 25 of 42	



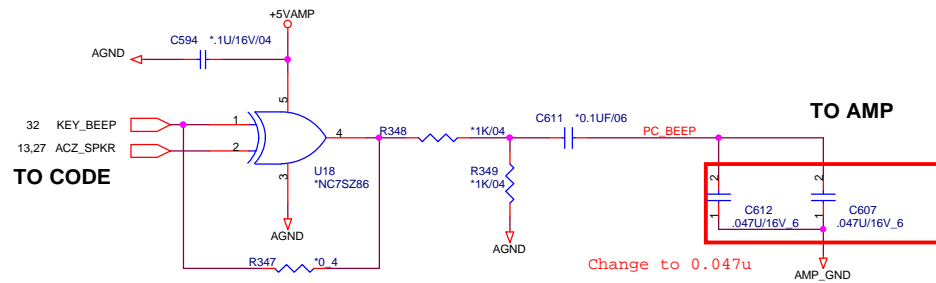


Audio JACK: Normal Open  
SA\_A# -->EXT HP  
SA\_B# -->EXT MIC  
Sense\_B -->INT MIC

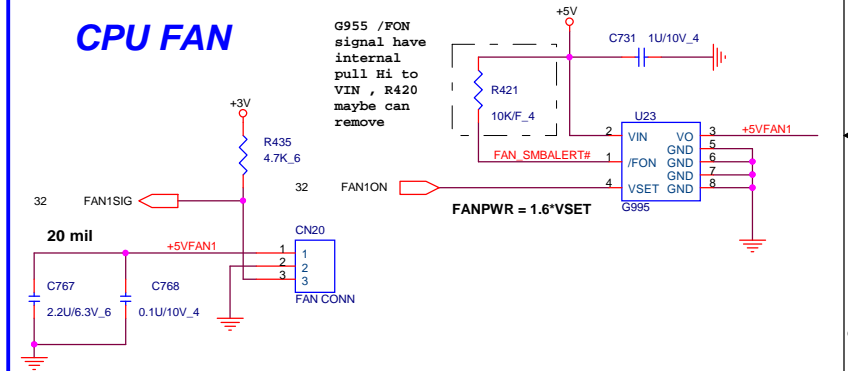




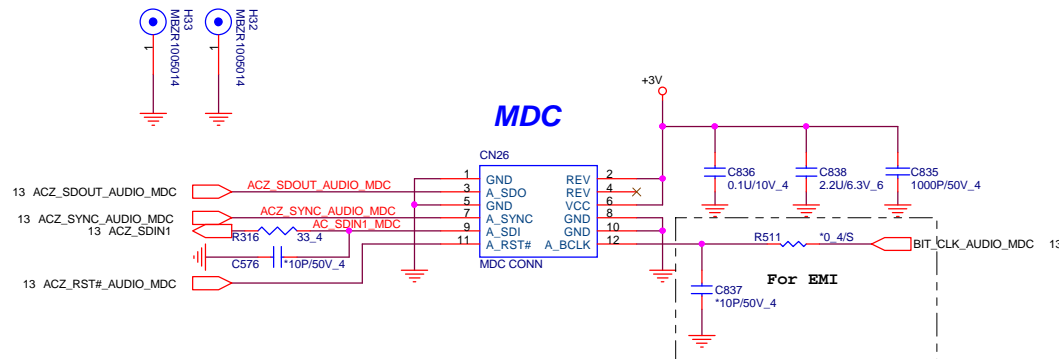
## PC-BEEP



## CPU FAN



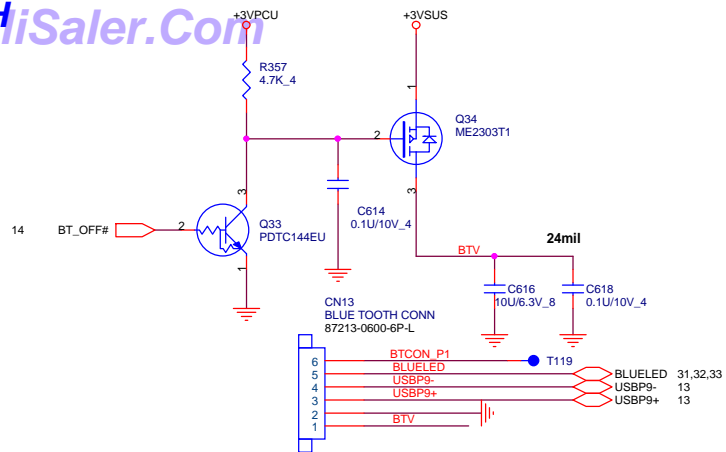
## Modem CONN



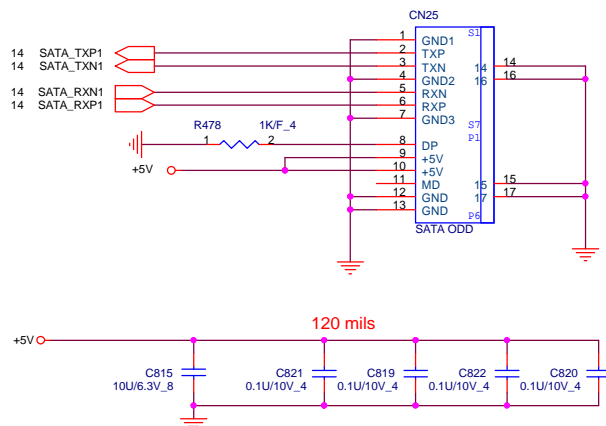
**PROJECT : OP8**  
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
	AMP_TPA6017/MDC1.5/CPU FAN	
Date: Friday, March 20, 2009	Sheet 28 of 42	

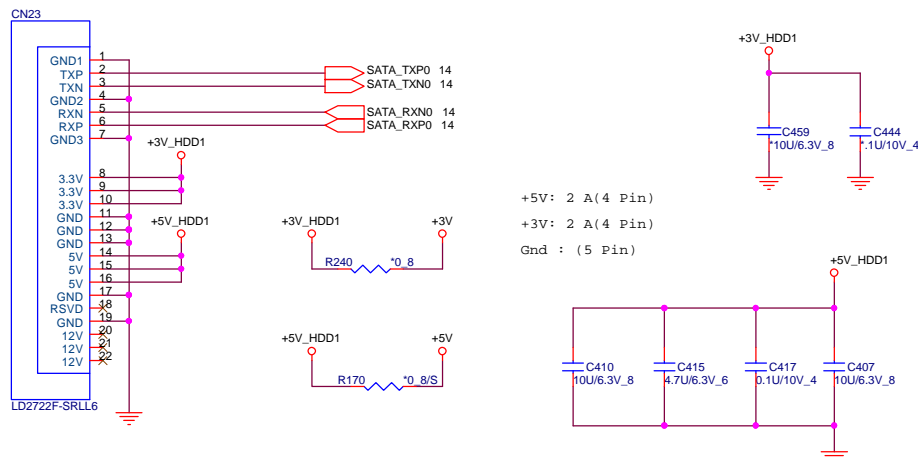




## SATA CD-ROM

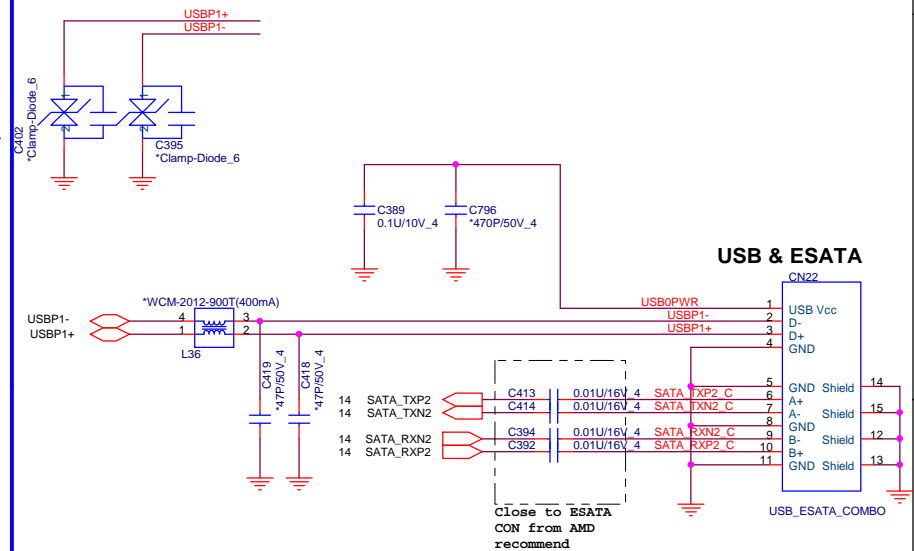
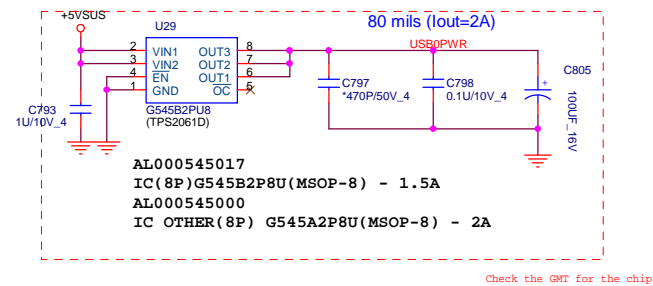


## SATA HDD

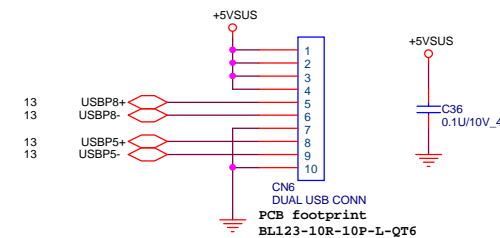


## LEFT SIDE USBX1 and E-SATA/USB COMBO

29

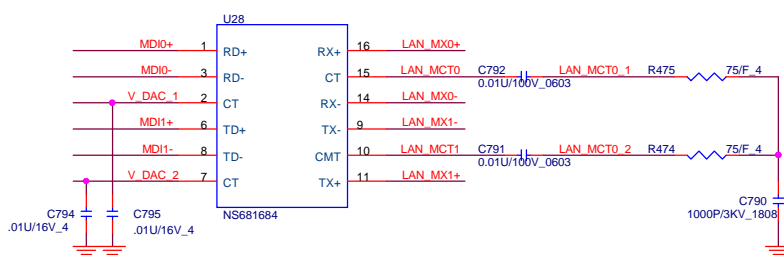
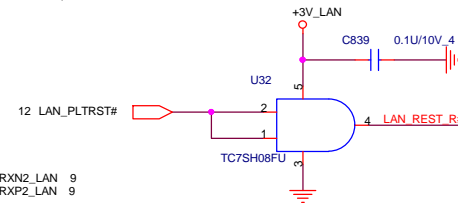
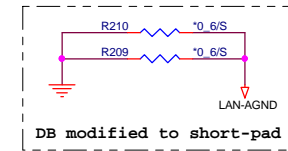
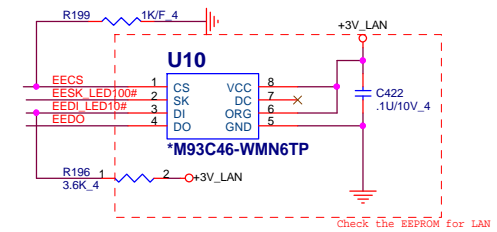
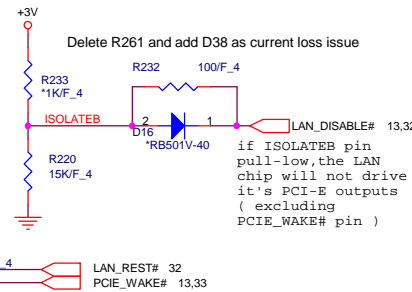
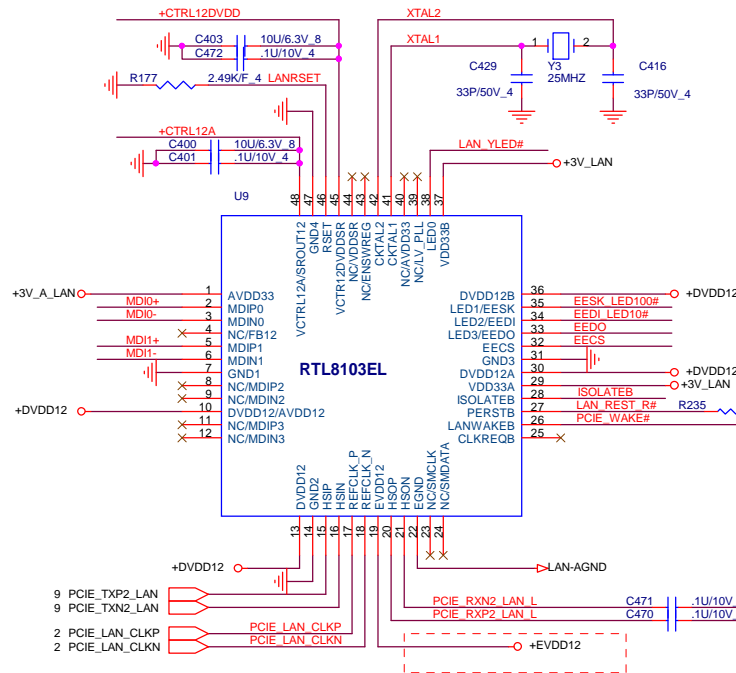
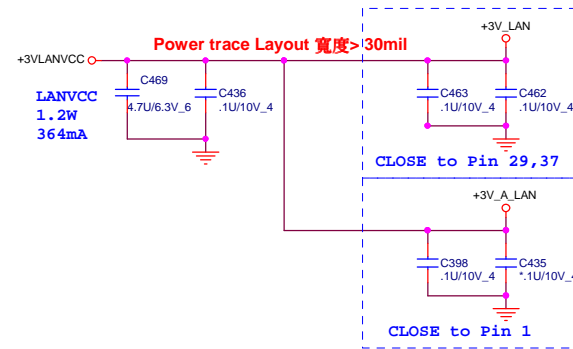
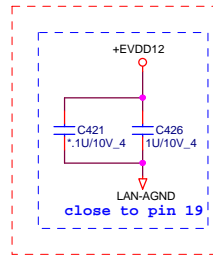
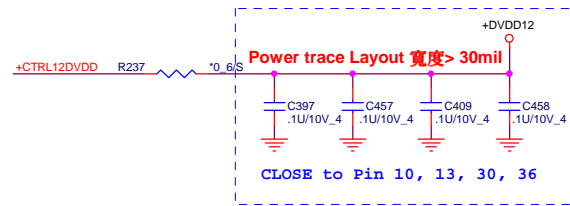


## RIGHT SIDE USBX2

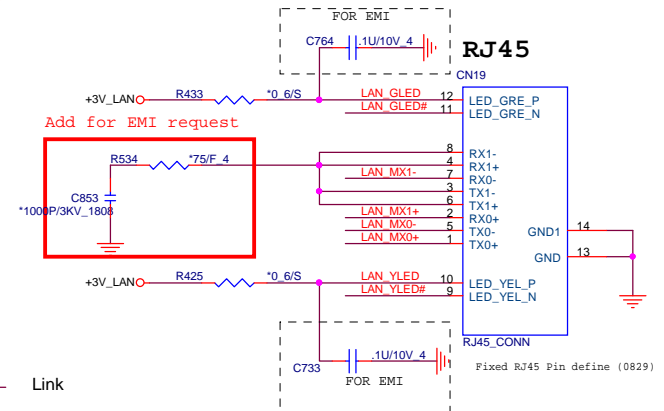
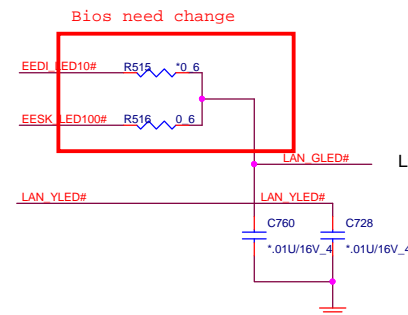


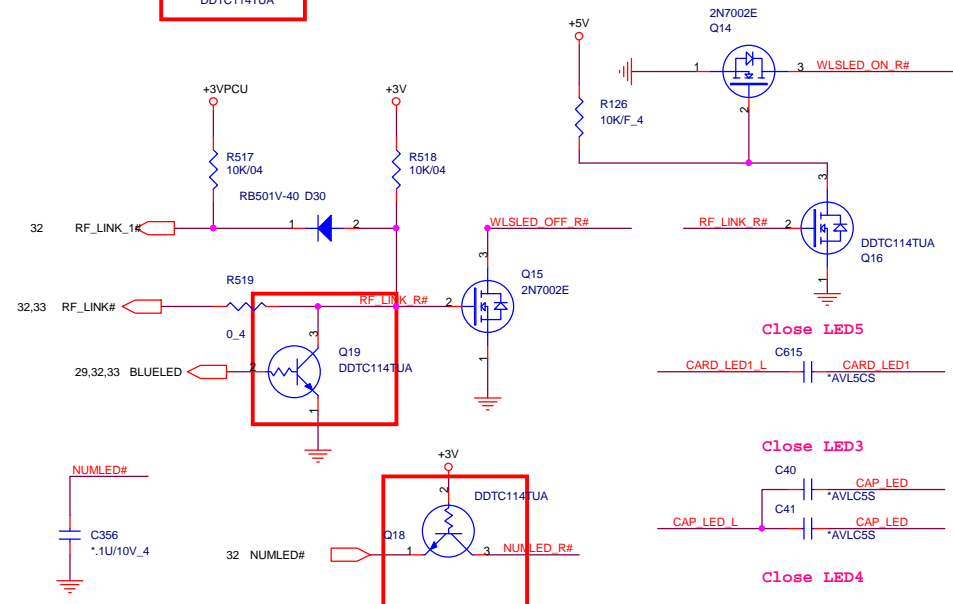
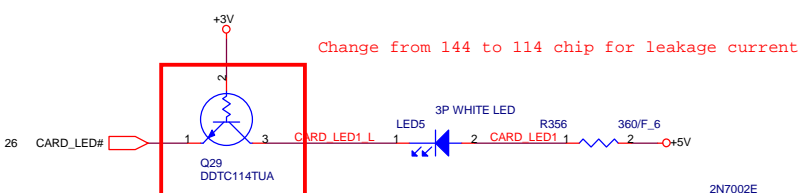
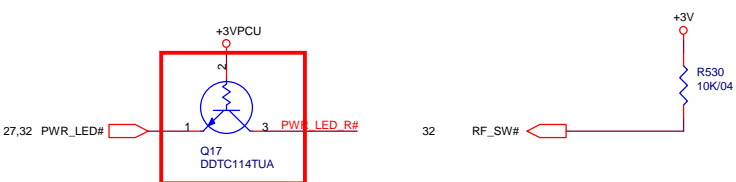
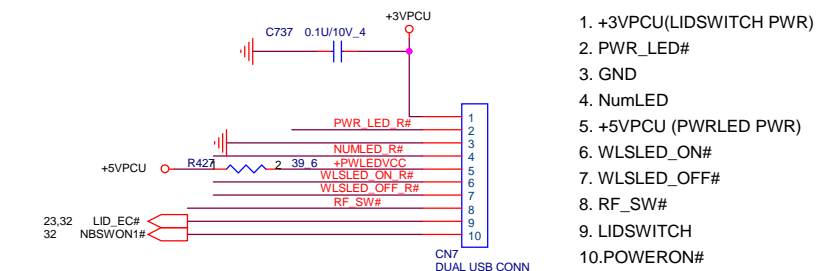
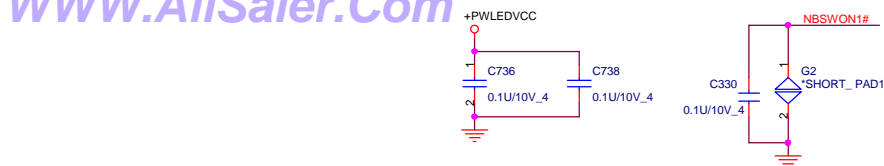
**PROJECT : OP8**  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BT/USBX3/ESATA/SATA ODD/HDD	1A
Date: Friday, March 20, 2009	Sheet 29 of 42	

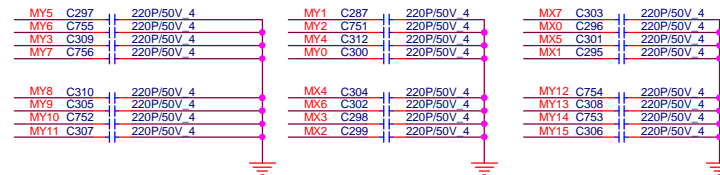


Symbol	Type	Pin No (64-Pin)	Pin No (45-Pin)	Description
LED0	O	57	38	LED0-0 00 01 10 11
LED1	O	56	35	LED0 Tx/Rx Tx/Rx Tx Tx
LED2	O	55	34	LED1 LINK100 LINK LINK LINK100
LED3	O	54	33	LED2 LINK10 FULL Rx LINK10
				LED3 NA NA NA NA

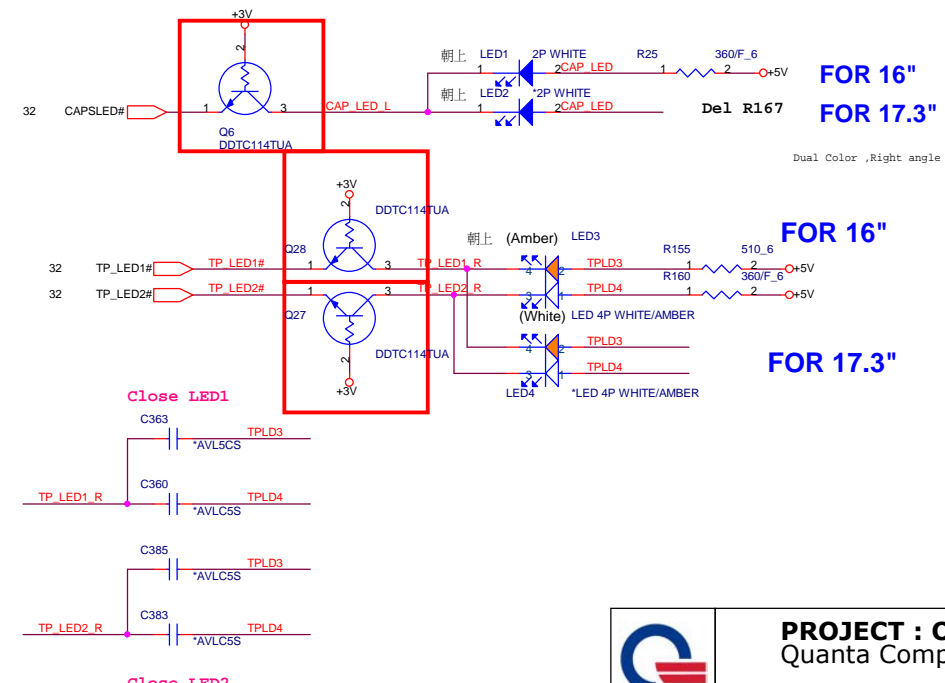
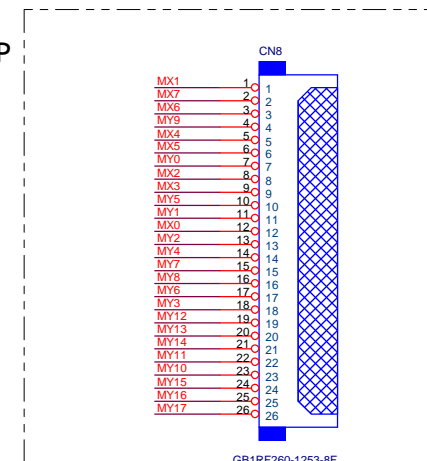
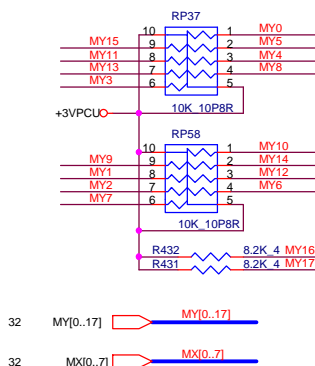


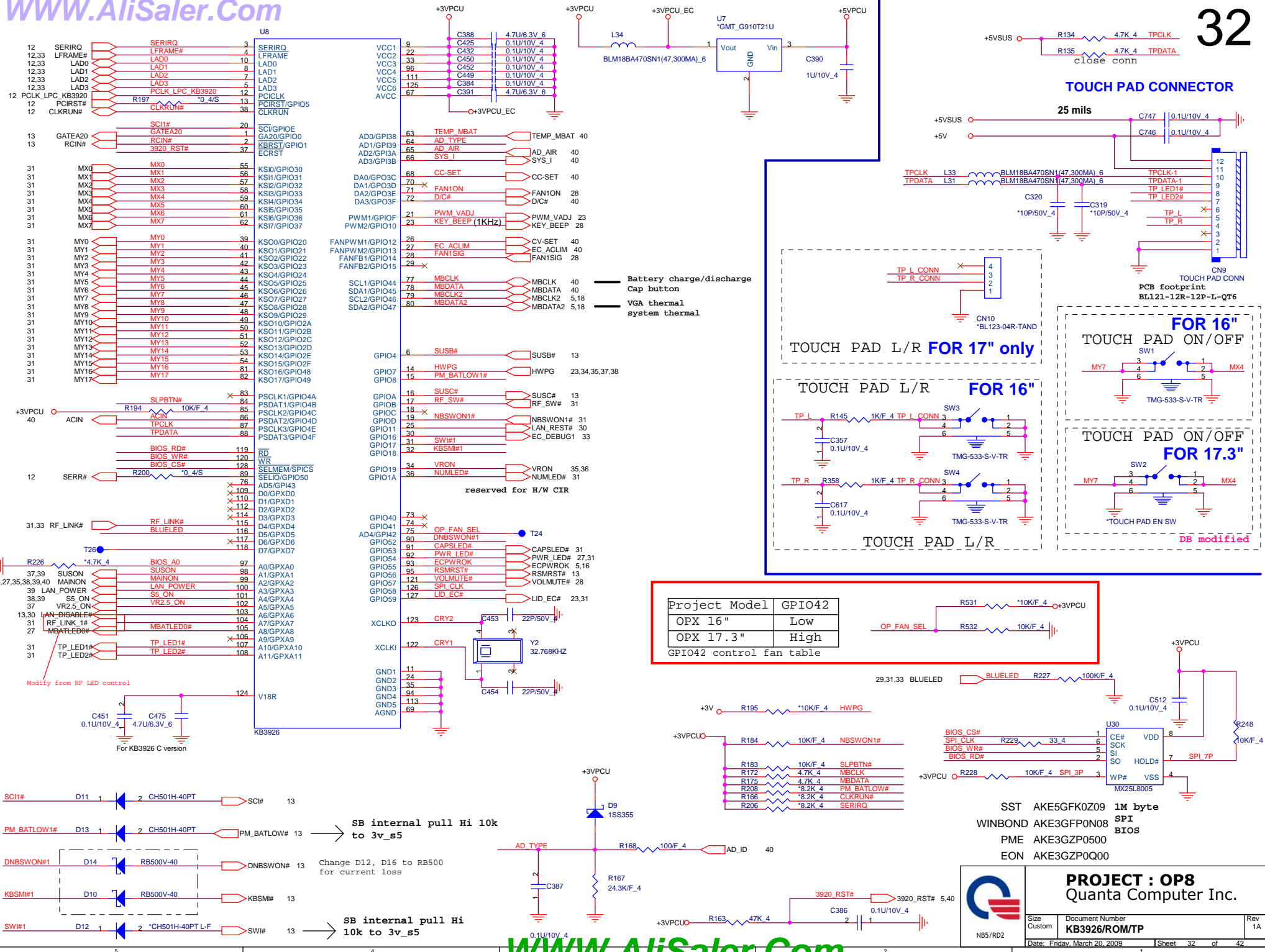


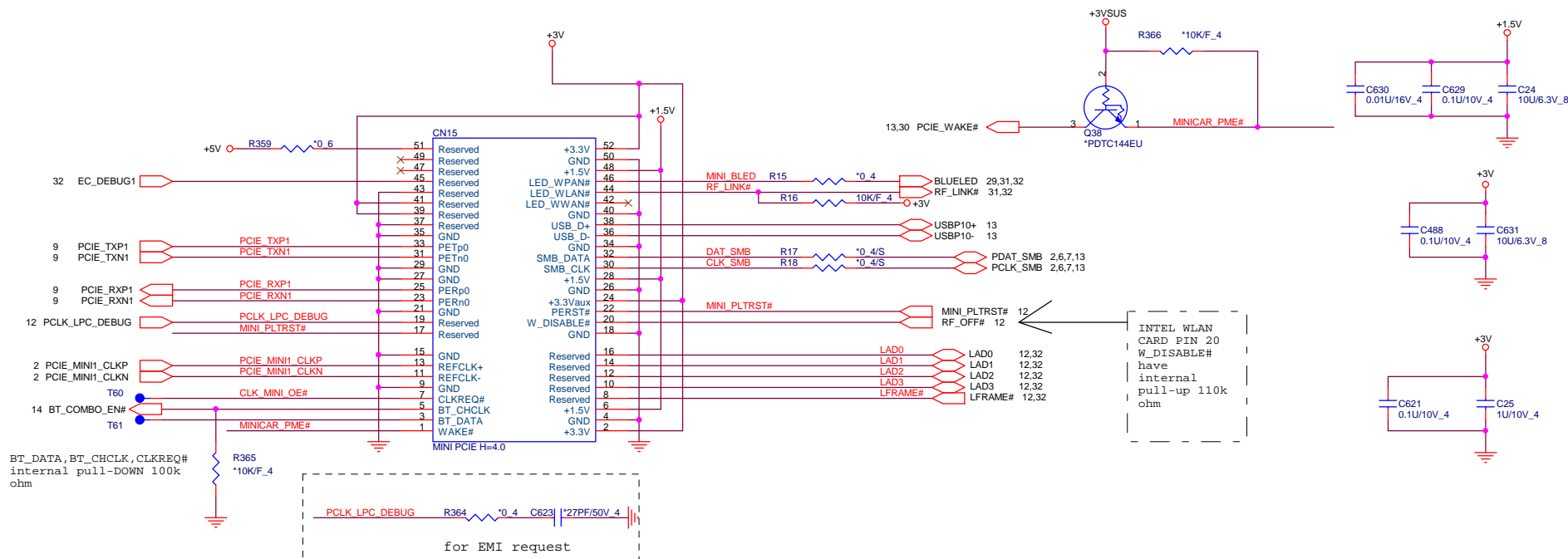
POWER BUTTON CONNECT

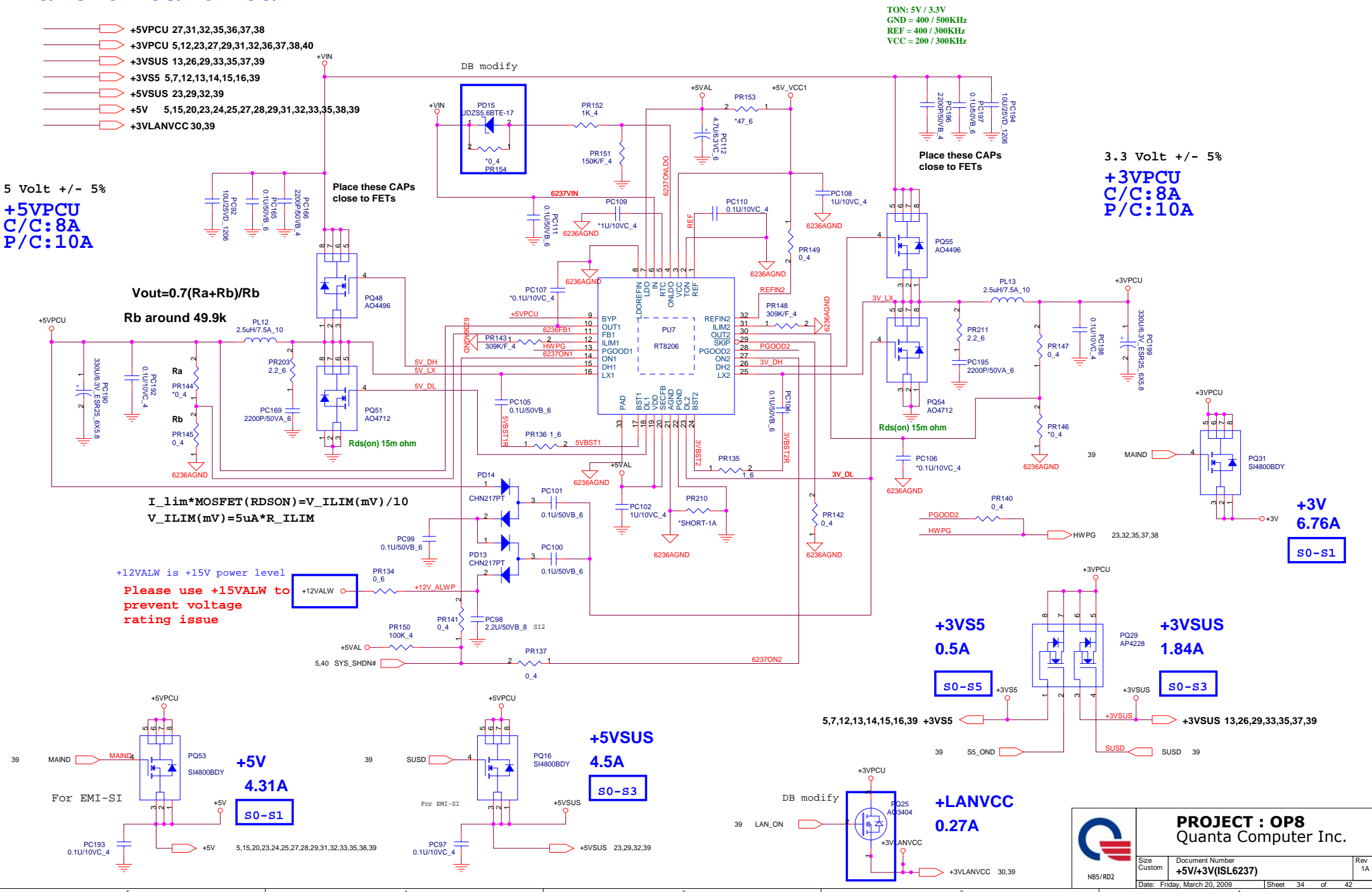


KEYBOARD PULL-UP









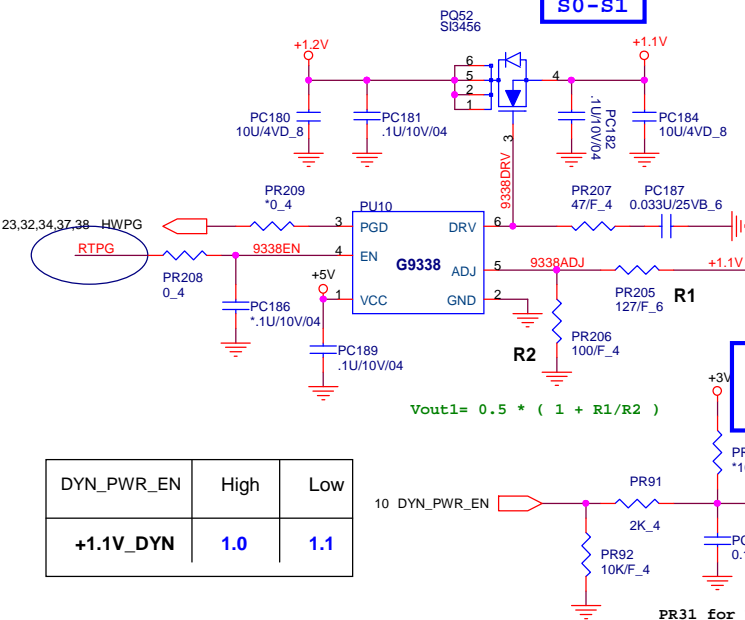


$$T_{on} = 3.85p \cdot R_{TON} \cdot V_{OUT} / (V_{IN} - 0.5)$$

$$Frequency = V_{out} / (V_{IN} \cdot T_{ON})$$

reserved for pwr seq -- andrew

3.82A  
S0-S1



+1.2V  
12A (4.3A+7.0A)  
S0-S1



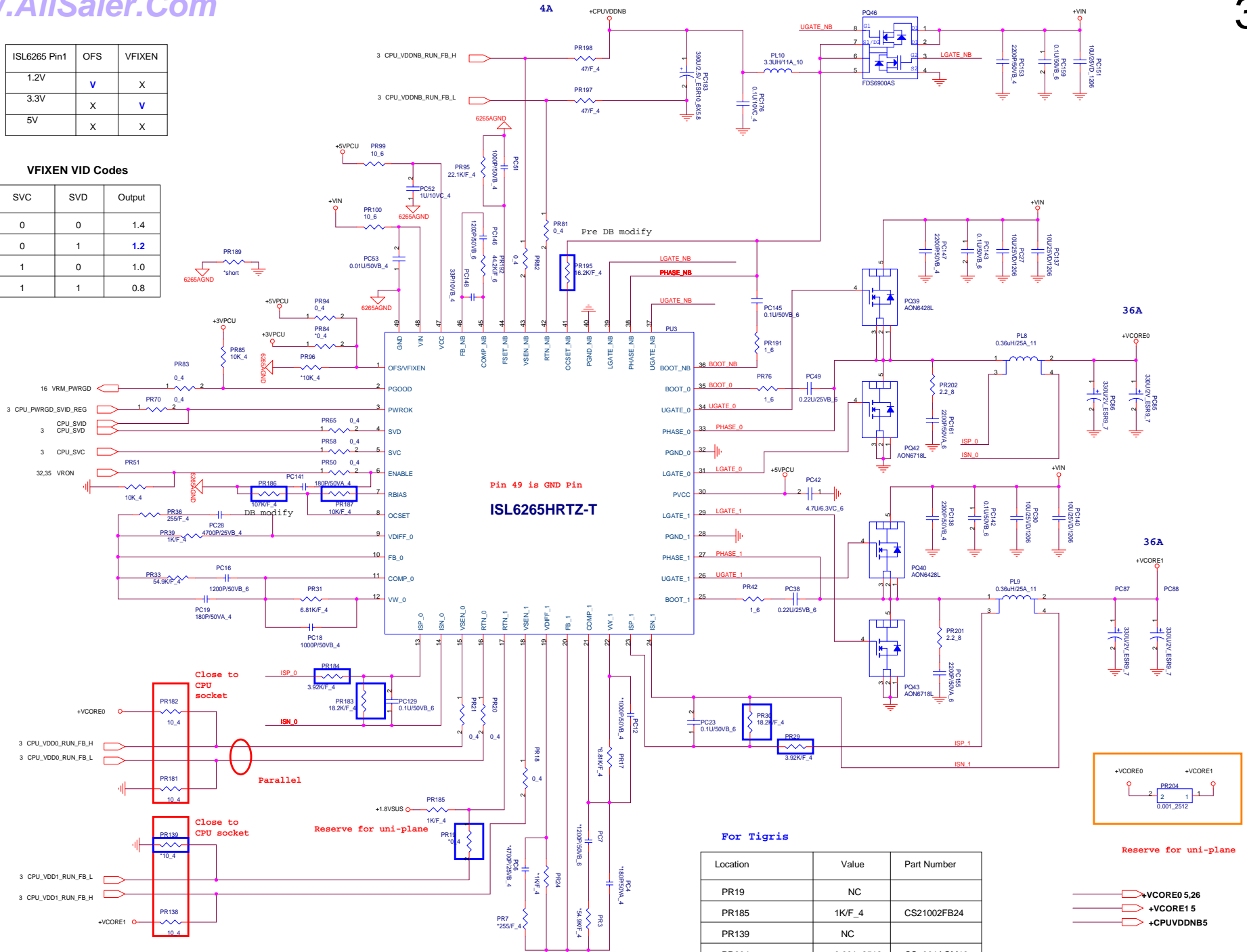
PROJECT : OP8  
Quanta Computer Inc.

Size B	Document Number <b>+1.2V &amp; +1.1V(RT8204)</b>	Rev 1A
Date: Friday, March 20, 2009	Sheet 35 of 42	

ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

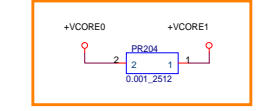
VFIXEN VID Codes

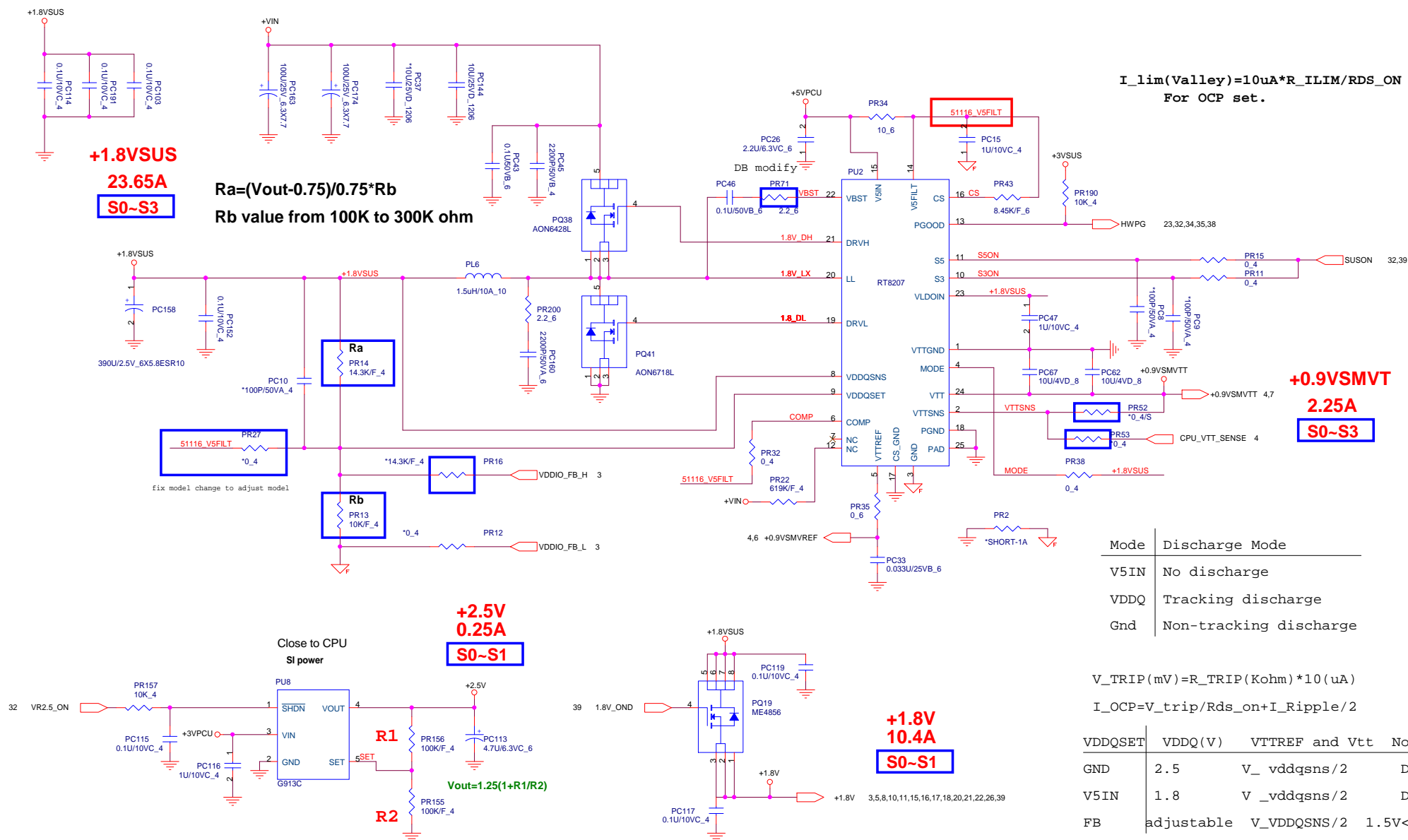
SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



For Tigris

Location	Value	Part Number
PR19	NC	
PR185	1K/F_4	CS21002FB24
PR139	NC	
PR204	0.001_2512	CS+001AGM13
PC12,PR17,PC4,PC7,PR3,PR24,PC6,PR7	NC	





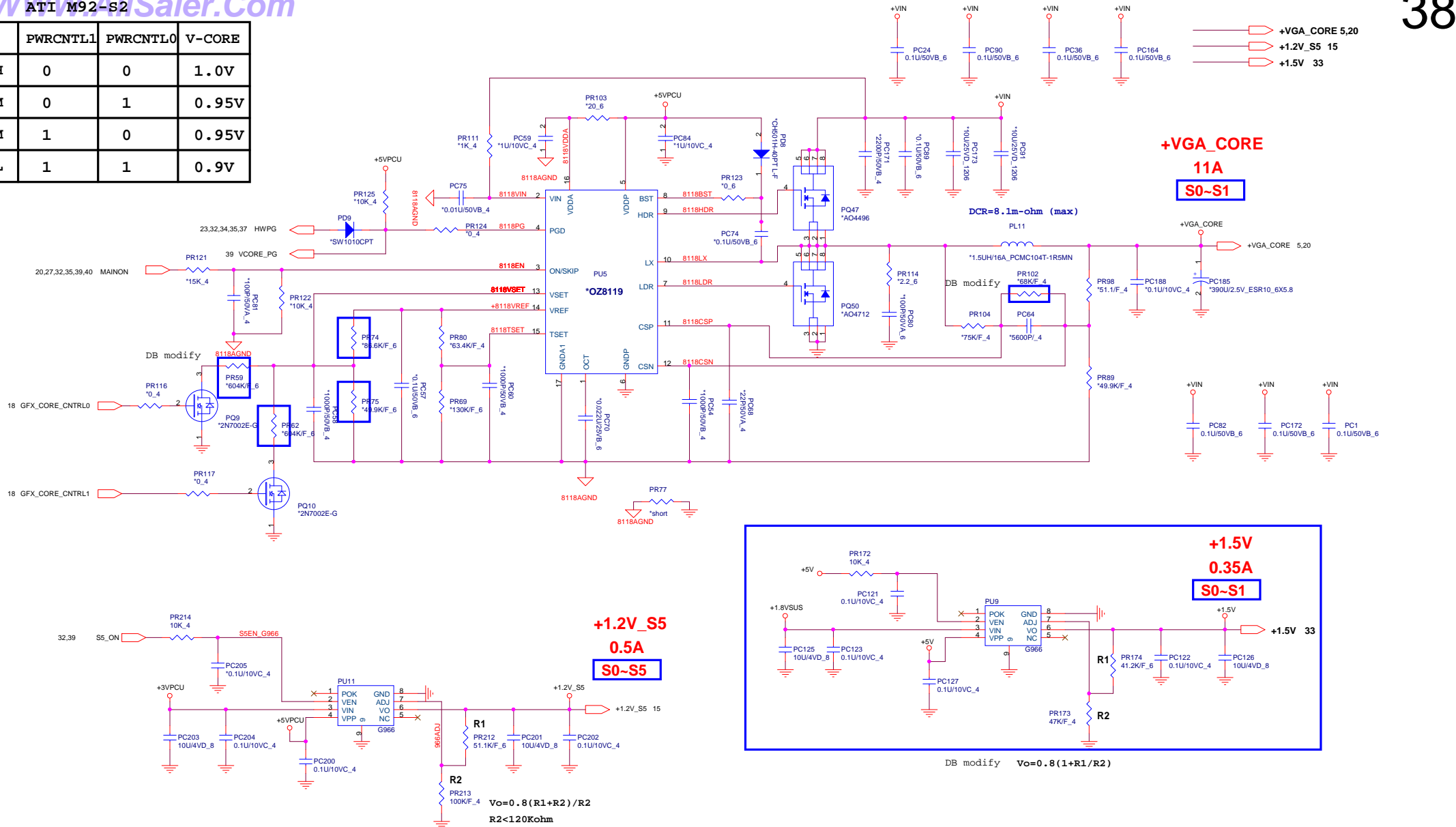
**Discrete:SI4856**  
**UMA:SI4800**

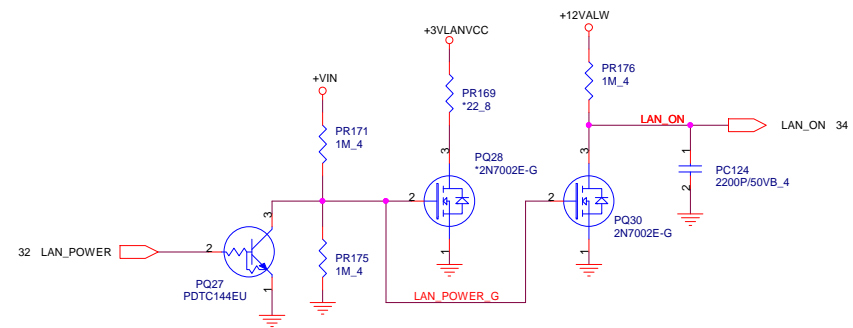
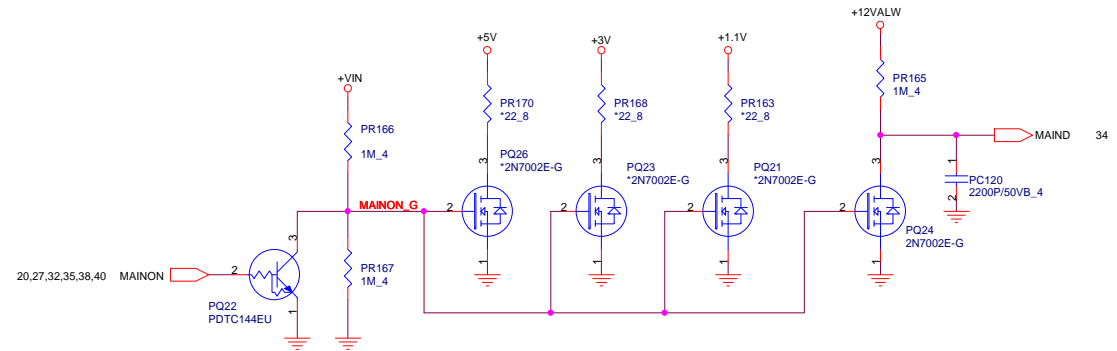
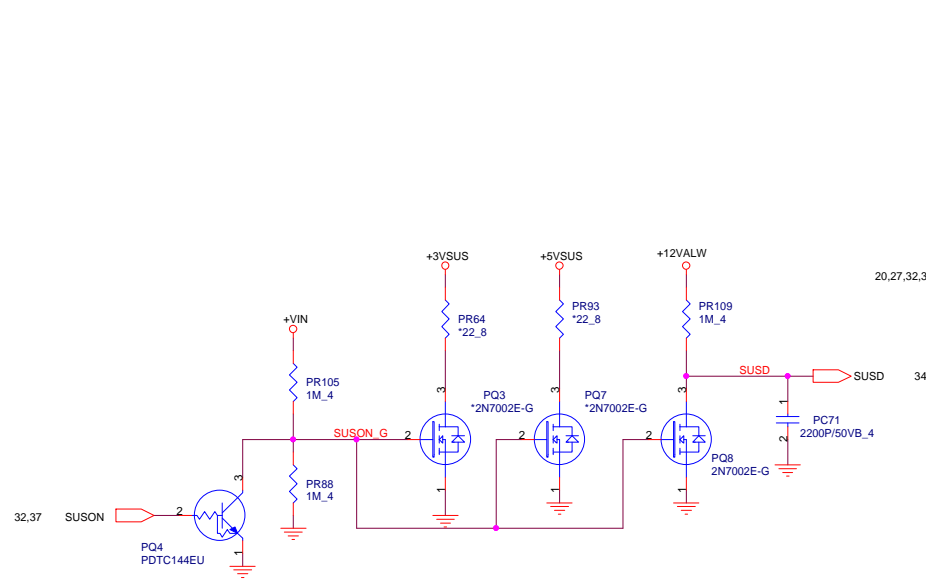


**PROJECT : OP8**  
Quanta Computer Inc.

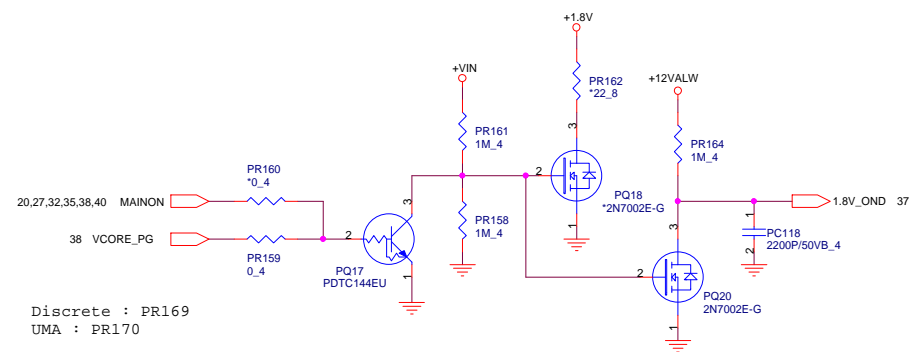
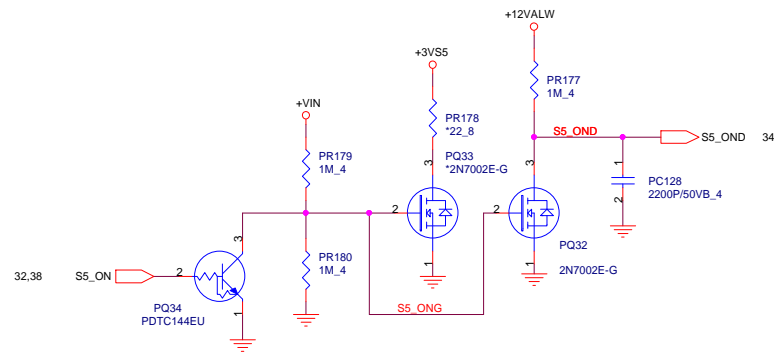
Size Custom	Document Number <b>1.8VSUS/DDR_VTER/+1.8V/2.5V</b>	Rev 1A
Date: Friday, March 20, 2009		Sheet 37 of 42

	PWRCNTL1	PWRCNTL0	V-CORE
H	0	0	1.0V
M	0	1	0.95V
M	1	0	0.95V
L	1	1	0.9V





For Discrete Only



Discrete : PR169  
UMA : PR170

